MAINTENANCE MANUAL

1998 AND 1999

1.3 GHz AND 2.6 GHz FREQUENCY COUNTERS

RACAL INSTRUMENTS LTD

RACAL

The Electronics Group

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1998 AND 1999

1.3 GHz AND 2.6 GHz FREQUENCY COUNTERS

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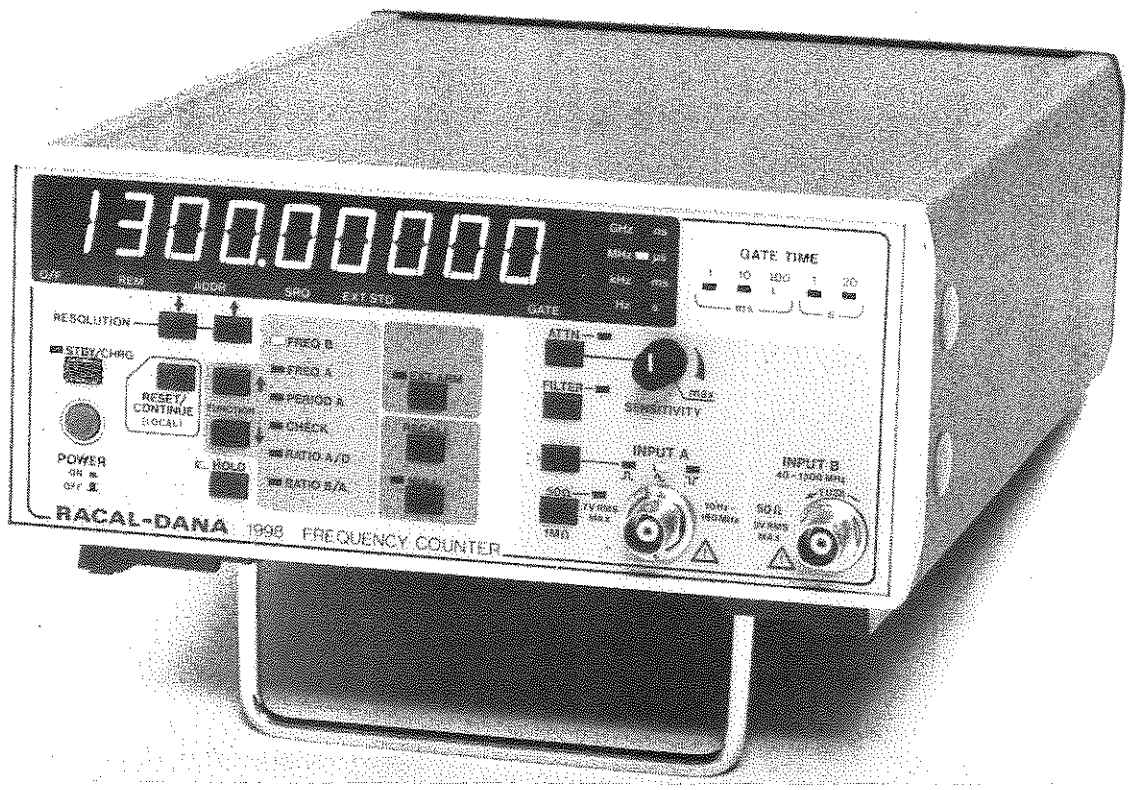
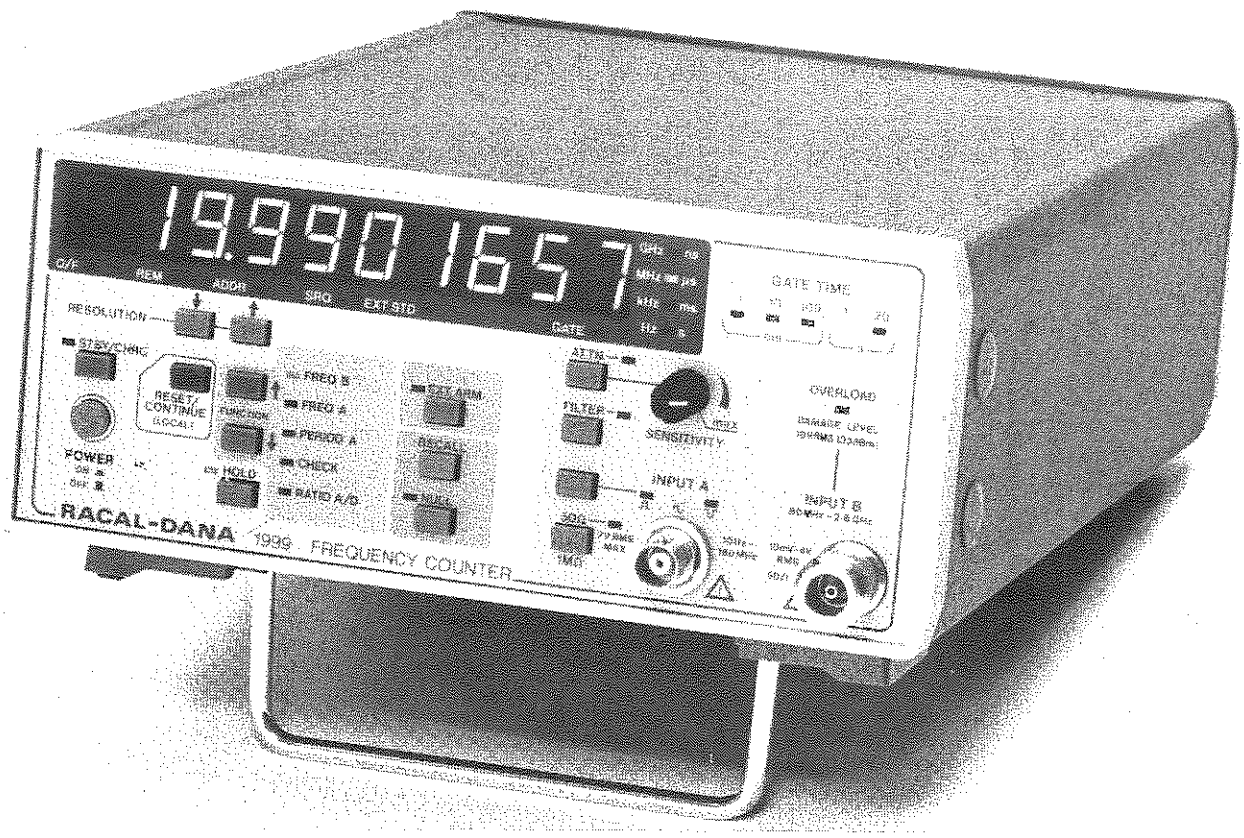


Frequency Counter 1998



RACAL

TH 8230

Frequency Counter 1999

LETHAL VOLTAGE WARNING

VOLTAGES WITHIN THIS EQUIPMENT ARE SUFFICIENTLY HIGH TO ENDANGER LIFE.

COVERS MUST NOT BE REMOVED EXCEPT BY PERSONS QUALIFIED AND AUTHORISED TO DO SO AND THESE PERSONS SHOULD ALWAYS TAKE EXTREME CARE ONCE THE COVERS HAVE BEEN REMOVED.

RESUSCITATION

TREATMENT OF THE NON-BREATHING CASUALTY

1 SHOUT FOR HELP. TURN OFF WATER, GAS OR SWITCH OFF ELECTRICITY IF POSSIBLE

Do this immediately. If not possible don't waste time searching for a tap or switch.

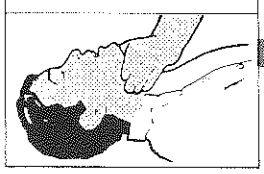
2 REMOVE FROM DANGER: WATER, GAS, ELECTRICITY, FUMES, ETC.

Safeguard yourself when removing casualty from hazard. If casualty still in contact with electricity, and the supply cannot be isolated, stand on dry non-conducting material (rubber mat, wood, linoleum).
Use rubber gloves, dry clothing, length of dry rope or wood to pull or push casualty away from the hazard.

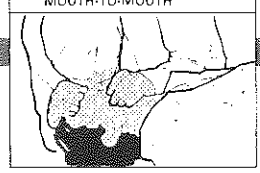
3 REMOVE OBVIOUS OBSTRUCTION TO BREATHING

If casualty is not breathing start ventilation at once.

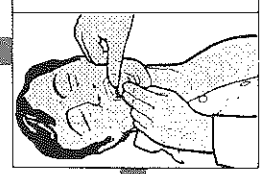
LOOSEN NECKWEAR
TILT HEAD BACKWARDS
AND PUSH CHIN UPWARDS



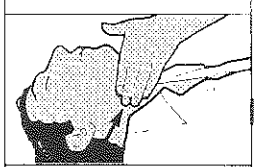
PINCH THE NOSE
COMMENCE VENTILATION
FOUR GOOD INFLATIONS
MOUTH-TO-MOUTH



IF CHEST DOES NOT RISE
RE-CHECK AIRWAY, REMOVE
OBSTRUCTION AND RE-INFLATE



CHECK PULSE



POSITION OF PULSE

PULSE PRESENT

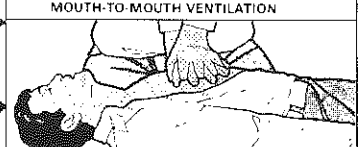
PULSE ABSENT

CONTINUE INFLATIONS
UNTIL RECOVERY OF
NORMAL BREATHING

HEART HAS STOPPED BEATING
LAY ON BACK ON FIRM SURFACE
(eg FLOOR).
COMMENCE EXTERNAL CHEST
COMPRESSION AND CONTINUE
MOUTH-TO-MOUTH VENTILATION

ONE FIRST AIDER
15 Compressions at 80 per minute followed by 2 Inflations

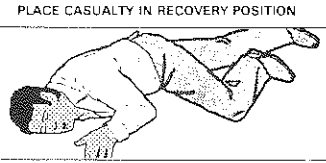
TWO FIRST AIDERS
One conducts chest compressions, without pause at 60 per minute. The other administers mouth-to-mouth ventilation – after each 5th compression.



Check heart beat after first minute and then after every three minutes. Continne external chest compression and mouth-to-mouth ventilation until a normal pulse is felt and colour improves.

CONTINUE INFLATIONS
UNTIL RECOVERY OF
NORMAL BREATHING

WHEN NORMAL BREATHING COMMENCES
PLACE CASUALTY IN RECOVERY POSITION



Keep casualty at rest. Remove on a stretcher. Watch closely, particularly for difficulty in breathing. Lightly cover with blankets or other materials.

SEND FOR DOCTOR AND AMBULANCE

DOCTOR	AMBULANCE	HOSPITAL	Nearest First Aid Post
TELEPHONE	TELEPHONE	TELEPHONE	

'POZIDRIV' SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trademark of G.K.N. Screws and Fasteners. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools.

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

MOS ELECTRONIC DEVICES

This unit contains MOS devices, and care should be taken to avoid static discharge damage.

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SECTION 1 TECHNICAL SPECIFICATION

Input Characteristics

Input A

Frequency Range	10Hz to 160MHz
Input Impedance (nominal)	
×1 attenuation	1 Megohm/40pF (AC coupled) or 50 ohms (DC coupled)
×20 attenuation	1 Megohm/25pF (AC coupled) or 50 ohms (DC coupled)
Dynamic Range	±1V pk (×1), ±20V pk (×20)
Sensitivity	
Sinewave	<10mV rms, 20Hz to 120MHz <50mV rms, 120MHz to 160MHz <20mV rms, 10Hz to 20Hz
Pulse	5nS min. pulse width (∿) 45mV pk-pk at 25% and 75% duty cycles (⎍/⎍) 28mV pk-pk at up to 10% duty cycles 45mV pk-pk at 25%/75% duty cycle
Input Attenuation Range	0dB to approx. 58dB in two ranges, continuously variable using sensitivity control and ×1/×20 attenuator control
Maximum Input (without damage)	
50 ohms	10V rms (DC coupled)
1 Megohm (×1 attenuation)	260V (DC + AC rms), from DC to 2kHz, decreasing to 10V rms at 50kHz and above.
1 Megohm (×20 attenuation)	260V (DC + AC rms) From DC to 40kHz, decreasing to over 10V rms at 1MHz and above.
Trigger Levels	Three selectable trigger levels are available to provide optimum triggering on waveforms with different duty cycles. (Sens control set to maximum, ×1 attn.)

	Offset	Trigger edge
(⎍)	+9mV	Negative
(∿)	0mV	Positive
(⎍)	−9mV	Positive

Filter	50kHz nominal low pass filter. Attenuation rate 20dB/decade nom.

Input B (Model 1998)

Frequency Range	40MHz to 1.3GHz, AC coupled
Input	50ohms nominal (BNC connector)
VSWR	⩽2:1 (1GHz)
Operating Range (sinewave)	<10mV to 5V rms to 1GHz <75mV to 5V rms to 1.3GHz
Maximum Input	7V rms (fuse protected).
Damage Level	25W

Input B (Model 1999)

Frequency Range	80MHz to 2.6GHz (3GHz under restricted operating conditions)
Input	50ohms nominal, AC coupled ('N' type connector)
VSWR	⩽2:1 to 2.6GHz (typically <1.5:1)
Operating Range (sinewave)	<10mV to 4V rms min. 80MHz to 2.6GHz
Overload	Protection/indication above 4V (min)
Damage Level	+33dBm, ±40V DC or pulsed.
AM Tolerance	⩾90% at 1.3GHz

Input D

	Used in Ratio A/D mode.
Frequency Range	10kHz to 10MHz usable down to 1kHz with reduced sensitivity.
Input Impedance (nominal)	1kohm for signals <1V p-p, decreasing to 500 ohm for signals ⩾10V p-p. (AC coupled.)
Input Signal Range (sinewave)	100mV to 10V rms, 10kHz to 10MHz. Typically 1V to 10V rms, 1kHz to 10kHz.
Damage Level	260V (DC +AC rms) up to 384 Hz decreasing to 10V rms above 10kHz.

External Arming

	External TTL timing signal can be applied to EXT ARM INPUT (rear panel).
Damage Level	10V rms or ±15V pk
Input Impedance	1 kohm nominal, (DC coupled)
Slope	Armed on positive edge
Slew rate	2V/μs min
Pulse Width	200nS min.
Set Up Time	100nS after input edge.

Measurement Modes

Frequency A and B

Range	
Frequency A	10Hz to 160MHz
Frequency B	40MHz to 1.3GHz (Model 1998) 80MHz to 2.6GHz (Model 1999)
Digits Displayed	3 to 10 digits
LSD Displayed (Hz)	$F \times 10^{-D}$ (F = Frequency rounded up to next decade, D = No. of digits).
Resolution* (Hz)	±n LSD† ±1.4 (Trigger Error* × Freq)/Gate Time
Accuracy* (Hz)	± Resolution ± (Timebase Error × Freq.)

Period A (Period Average)

Range	6.25nS to 100mS
Digits Displayed	3 to 10 digits
LSD Displayed (Sec)	$P \times 10^{-D}$ (P = Period rounded up to next decade, D = No. of digits).
Resolution *(Sec)	±n LSD† ±1.4 (Trigger Error* × Period)/Gate Time
Accuracy *(Sec)	± Resolution ± (Timebase Error × Period).

† n = 1 for 3-5 and 10 digits or 2 for 6-9 digits
* See Definitions

1998/99
FD 459

Ratio B/A (Model 1998 Only)

Specified for higher frequency applied to input B

Range

Input A	10Hz to 100MHz
Input B	40MHz to 1.3GHz
LSD Displayed	1 to 8 digits determined by Freq A and gate time selected
Resolution*	±LSD ±1.4 (Trigger Error (A)* × Ratio)/Gate Time
Accuracy*	±Resolution

Ratio A/D

Specified for higher frequency applied to input A

Range

Input A	10Hz to 100MHz
Input D	1kHz to 10MHz
LSD Displayed	1 to 8 digits determined by Freq D and gate time selected
Resolution*	±LSD ±1.4 (Trigger Error (A)* × Ratio)/Gate Time
Accuracy*	±Resolution

Burst

Min Burst time 1mS + Gate Time*

General

Internal Timebase

Crystal Controlled

Frequency	10MHz
Aging Rate	2×10^{-6} in the first year
Temperature Stability	$\pm 1 \times 10^{-5}$ over the range 0° to 50°C.
Adjustment	Via rear panel

Frequency Standard Output

Frequency	10MHz
Amplitude	TTL levels giving approx. 1V p-p into 50 ohms.
Impedance	90 ohms nominal.
Max. Reverse Input	±15V

External Standard Input

Frequency	10MHz (see also Option 10 for other frequencies). See Input D for further specifications.

Gate Time Automatically determined by number digits selected. LED annunciators indicate gate time.

No. of Digits Selected	Gate Time (Seconds)
10	20
9	1
8	0.1
7	0.01
6,5,4,3	0.001

These nominal gate times will be extended depending on period of input signal (see definitions).

Gate Output	Available as a TTL compatible signal at the rear panel.

Single Cycle (Hold) Enables a single measurement to be initiated and held.

Display 10 digit high brightness, 14mm LED display.

Power Requirements

Voltage	90-110 103-127 193-237 212-265 } (externally selectable)
Frequency	45-440Hz
Rating	25VA typically.

Operating Temperature Range 0° to +50°C (0° to +40°C with battery pack).

Storage Temperature Range −40°C to +70°C (−40°C to +60°C with battery pack).

EMC/RFI MIL-STD-461B

Environmental Designed to meet MIL-T-28800 and DEF-STD-66/31

Safety Designed to meet the requirements of IEC 348 and follow the guidelines of UL1244.

Weight Net 3.6kg (8lb) excluding battery
6.8kg (15lb) including battery
Shipping 5.5kg (12lb) excluding battery
8.7kg (19lb) including battery

Normal Dimensions See back page

Shipping Dimensions 430 × 360 × 280mm (16.91 × 14.2 × 11.0 in)

Options

Options 04T

Temperature Compensated Crystal Oscillator

Frequency	10MHz
Aging Rate	3×10^{-7}/month 1×10^{-6} in the first year
Temperature Stability	$\pm 1 \times 10^{-6}$ over the range 0°C to +40°C (operable to +50°C)

Option 04A

Ovened Oscillator

Frequency	10MHz
Aging Rate	3×10^{-9}/day averaged over 10 days after 3 months continuous operation.
Temperature Stability	$\pm 3 \times 10^{-8}$/°C averaged over range 0°C to +45°C (operable to +50°C)
Warm Up	Typically $\pm 1 \times 10^{-7}$ within 6 minutes.

† n = 1 for 3-5 and 10 digits or 2 for 6-9 digits
* See Definitions

Option 04B

High Stability Ovened Oscillator

Frequency	10MHz
Aging Rate	5×10^{-10}/day averaged over 10 days after 3 months continuous operation.
Temperature Stability	$\pm 6 \times 10^{-10}$/°C averaged over range 0°C to +45°C (operable to +50°C)
Warm Up	$\pm 1 \times 10^{-7}$ within 20 minutes

Option 07.

Rechargeable Battery Pack and External DC Operation

Battery Type	Sealed lead-acid cells
Battery Life (at 25°C)	Typically 5 hours (24 hrs on standby) – 1998 Typically 3.75 hours (12 hrs on standby) – 1999
Battery Condition	Display indicates battery low
External DC	11-16V via socket on rear panel (–ve ground, not isolated).

Option 10

Reference Frequency Multiplier

Input Frequency	1,2,5 or 10MHz ($\pm 1 \times 10^{-5}$)

Option 55

GPIB Interface	Complies with IEEE-STD-488 (1978) and to conform with the guidelines of IEEE-STD-728 (1982).
Control Capability	All functions/controls programmable except power on/off, standby/charge and sensitivity potentiometer.
Output	Engineering format (11 digits and exponent)
IEEE-STD-488 Subsets	SH1, AH1, T5, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E2.
Handshake Time	250 μS to 1mS/character dependent on message content.
Read Rate	Typically 18/sec dependent upon measurement function.

Definitions

† **LSD** (Least Significant Digit)
In frequency and Period modes display automatically upranges at 1.1 × decade and downranges at 1.05 × decade, except on Input B for input frequency >1GHz. Above 1GHz no ranging on 1998. Model 1999 upranges at 1.25GHz and downranges at 1.3GHz. Accuracy and Resolution expressed as an RMS value.

* **Trigger Error** RMS

$$\text{Trigger Error} = \frac{\sqrt{(e_i^2 + e_n^2)}}{S}$$

Where e_i = input amplifier RMS noise (typically 150μV RMS in 160MHz bandwidth)
e_n = input signal RMS noise in 160MHz bandwidth
S = Slew rate at trigger point V/Sec.

Gate Time

The gate time will be extended as below.

Function	Gate Time extended by
Freq. B	64 periods (1998) 256 periods (1999)
Freq. A, Period A (∿)	2 periods
Freq. A, Period A (⊓, ⊔)	1 period
Ratio B/A, A/D	1 period of Input A

Supplied Accessories

Power Cord
Spare Fuse
Operator's Manual
Spare 1.3GHz Fuse (Model 1998 Only)

Ordering Information

1998	1.3GHz Frequency Counter
1999	2.6GHz Frequency Counter

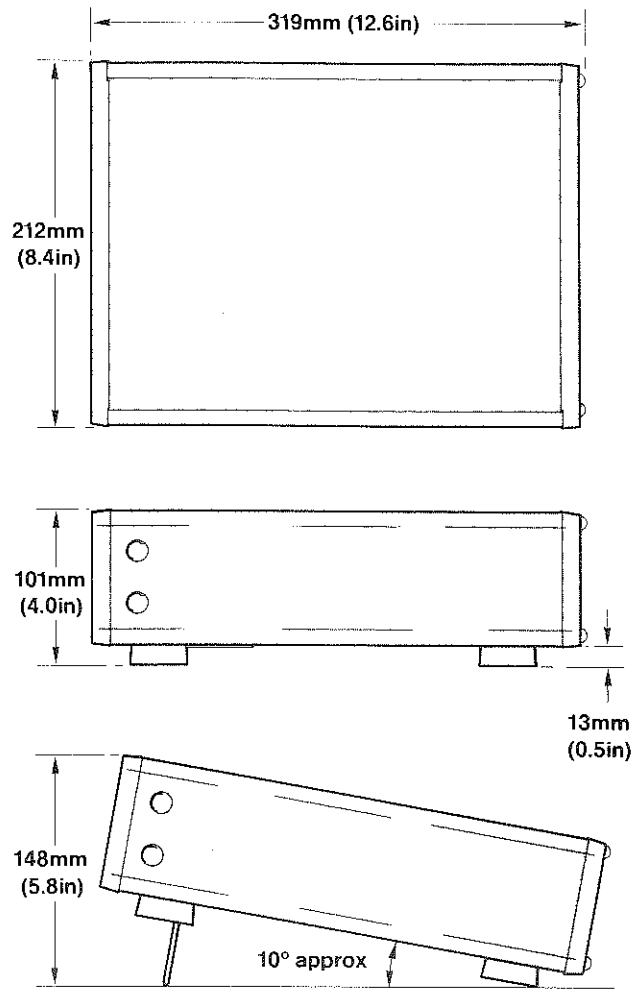
Options and Accessories

01*	Rear Panel Inputs (1998/1999)	11-1734/1735
04T**	TCXO	11-1713
04A**	Oven Oscillator	11-1710
04B**	High Stability Oven Oscillator	11-1711
07†	Battery Pack	11-1625
10	Reference Frequency Multiplier	11-1645
55†	GPIB Interface	11-1724
60	Handles	11-1730
60A	Rack Mounting Kit (Fixed Single)	11-1648
60B	Rack Mounting Kit (Fixed Double)	11-1649
61	Carrying Case	15-0773
61M	Protectomuff Case	15-0736
65	Chassis Slides (incl. Rack Mounts)	11-1716
	Telescopic Antenna	23-9020
	High Impedance 100 MHz Probe	23-9104
	1.3GHz Fuse (Pkt. 5) Model 1998 Only	11-1718

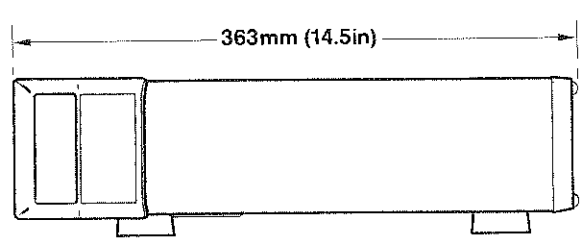
† The battery pack and GPIB options cannot both be fitted.

** Only one frequency standard may be fitted at any one time. The standard reference will be supplied unless option 04T, 04A or 04B is specified.

* Fitting Option 01 may affect certain specification parameters.



With Optional Handles Fitted



SECTION 2 GENERAL DESCRIPTION

INTRODUCTION

1 The Racal-Dana frequency counters Models 1998 and 1999 are microprocessor-controlled instruments offering high-accuracy measurements with a comprehensive range of facilities.

MEASURED FUNCTIONS

Frequency A Function

2 The Frequency A function is used to measure the frequency of the signal applied to the channel A input. A resolution of nine digits is available with a one-second gate time.

Frequency B Function

3 The Frequency B function is used to measure the frequency of the signal applied to the channel B input. A resolution of nine digits is available with a one-second gate time.

Period A Function

4 The Period A function is used to measure the period of the waveform applied to the channel A input. A number of periods, depending upon the resolution (and therefore the gate time) selected, are measured, and the average value is displayed.

Ratio A/D Function

5 The Ratio A/D function is used to measure the ratio of the frequency applied to the channel A input to that applied to the channel D input.

Ratio B/A Function (1998 Only)

6 The Ratio B/A function is used to measure the ratio of the frequency applied to the channel B input to that applied to the channel A input.

CHECK FUNCTION

7 With the Check function selected a number of functional tests of the instrument's circuits can be made without the use of additional test equipment. Although these tests do not check the instrument's performance to its published specification, they can be used to verify that the equipment is operating correctly. A suitable functional check procedure is given in Section 3.

SIGNAL INPUT CHANNELS

8 Signal input channels A and B are fully independent.

9 Channel A is provided with controls to permit the selection of:

(1) 1 MΩ or 50 Ω input impedance.

(2) Input attenuation continuously variable from 0 dB to approximately 58 dB using the ATTN (X20) and SENSITIVITY controls.

(3) 50 kHz low-pass filter.

(4) Pulse offset (trigger level) to cater for signals of various duty cycles.

10 Channel B has a 50 Ω input impedance. On the 1998 the input is fuse-protected for signals above 7 V. On the 1999 the input is protected by an internal attenuator for signals above 4 V.

ERROR INDICATION

11 Certain errors in the operation of the instrument will result in the generation of error codes, which will be displayed. Details are given in Section 4 of this manual.

EXTERNAL ARMING

12 External arming of the start circuit for the measurement interval can be carried out by means of signals connected to a BNC connector mounted on the rear panel.

DISPLAY

13 A 10-digit numeric display with units annunciators is used. Indicators are provided to show when overflow of the most significant digit occurs, and to show the measurement interval (gate time).

HOLD FEATURE

14 The hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

RESOLUTION AND GATE TIME

15 The gate time is determined by the display resolution selected. Details of the relationship between gate time and display resolution for each measurement mode are given in Section 4 of this manual.

GATE OUTPUT

16 The internally-generated gate signal is available at a pin on the rear panel. The gate output will be delayed relative to the internal measurement gate by 10 nsec typically (15 nsec maximum).

17 When used in the single-shot mode, the gate waveform comprises a short trigger pulse, followed by a hold-off time of about 1 ms followed by the measurement gate waveform proper; this is to allow the external circuit output to stabilise after triggering.

EXTERNAL FREQUENCY STANDARD INPUT

18 The instrument may be operated using an external frequency standard. The instrument will operate from the external standard, in preference to the internal standard, whenever the signal at the EXT STD INPUT socket is of sufficient amplitude. It will revert to operation from the internal standard automatically if the input from the external standard is removed.

STANDBY MODE

19 When the instrument is switched to standby, the internal frequency standard continues to operate and the instrument status is maintained but the measuring circuits are switched off. If the battery pack option is fitted and an external power supply is connected, the battery is charged at the full rate.

NULL FUNCTION

20 With the NULL function active the instrument displays the difference between the measured value and the value held in the internal NULL store.

INITIALIZATION

21 When the instrument is first switched on, or when it is initialised via the GPIB, it is set to the following conditions:

Measurement Function	FREQ A
Display Resolution	8 digits (0.1 second gate time)
Channel A Input	1 MΩ input impedance No trigger offset (∿) LF filter disabled X1 attenuation
Null Function Null Store	Disabled 0
External Arming	Disabled
Hold Function	Disabled

OPTIONS AVAILABLE

Frequency Standards (04X Options)

22 A wide range of internal frequency standard options is available. The technical specifications are given in Section 1 of this manual. The frequency standard can be changed, if required, by the customer: instructions are given in Section 3.

Reference Frequency Multiplier (Option 10)

23 The reference frequency multiplier is an internally-mounted, phase-locked multiplier, which permits the use of external frequency standard signals at 1 MHz, 2 MHz, 5 MHz or 10 MHz. The multiplier can be fitted by the customer: instructions are given in Section 3.

GPIB Interface (Option 55)

24 An internally mounted interface to the IEEE-488-GPIB is available. This permits remote control of all the instrument's functions except the power ON/OFF switching, the standby switching, and the channel A sensitivity potentiometer setting. The interface can be fitted by the customer: instructions are given in Section 3. The GPIB interface cannot be fitted to an instrument already fitted with the battery pack option. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an accessory.

Battery Pack (Option 07)

25 Fitting the internal Battery Pack Assembly permits the instrument to be used in locations where no suitable AC supply is available. The option also allows operation from an external DC supply.

26 The battery is trickle-charged whenever the instrument is operated from an AC supply and the internal/external switch is at INTERNAL BATTERIES. Charging at the full rate is carried out when the instrument is switched to the standby mode and connected to an external AC or DC supply. A full charge requires approximately 14 hours.

27 The instrument will operate continuously from a fully-charged battery for approximately 4.5 hours (1998) and 3.75 hours (1999). It will switch off automatically when the battery reaches the discharged condition. The STBY/CHRG indicator starts to flash approximately 15 minutes before this occurs. The battery life can be extended by use of the Battery-Save facility.

28 The battery pack can be fitted by the customer. Instructions are given in Section 3. When using the GPIB interface option the battery pack cannot be fitted.

Rack Mounting Kits

29 The following kits permitting the instrument to be mounted in a standard 19-inch rack are available:

(1) Single instrument, fixed-mount kit (Option 60A).
(Racal-Dana part number 11-1648).
The mounted instrument occupies half the rack width and is two rack units (3.5 inches) in height. The instrument is mounted offset in the rack and may be at either side.

(2) Double instrument, fixed-mount kit (Option 60B).
(Racal-Dana part number 11-1649).
The panel of the mounting kit occupies the full rack width and is two rack units (3.5 inches) in height. Two instruments can be mounted side-by-side.

30 All the kits can be fitted by the customer. Instructions are given in Section 3.

SECTION 3 PREPARATION FOR USE

UNPACKING

1 Unpack the instrument carefully to avoid unnecessary damage to the factory packaging.

2 If it becomes necessary to return the instrument to Racal-Dana Instruments for calibration or repair, the original packaging should be used. If this is not possible, a strong shipping container should be used. Ensure that sufficient internal packing is used to prevent movement of the instrument within the container during transit.

POWER SUPPLY

AC Line Voltage Setting

3 Before use, check that the AC voltage selector is set correctly for the local AC supply. The voltage range already set can be seen through a window in the selector board retaining clamp to the left of the AC power plug.

4 If it is necessary to change the setting, proceed as follows:

(1) Undo the selector board retaining clamp on the rear panel.

(2) Withdraw the board.

(3) Replace the board with the required voltage setting positioned so that it will show through the window in the retaining clamp.

(4) Replace the retaining clamp.

Line Fuse

5 Check that the rating of the line fuse is suitable for the AC voltage range in use. The fuse should be of the ¼ in x 1¼ in, glass cartridge, surge-resisting type. The required rating is:

90 V to 127 V: 500 mAT (Racal-Dana part number 23-0052).
188 V to 265 V: 250 mAT (Racal-Dana part number 23-0056).

Power Cord

6 The 1998/99 is a Safety Class 1 instrument, and is designed to meet international safety standards. A protective ground terminal, which forms part of the power-input connector on the rear panel, is provided. The instrument is supplied with a 3-core power cord. Only the power cord supplied should be used to make electrical connection to the power-input connector.

7 AC power for the instrument must be taken from a power outlet incorporating a protective ground connector. Whem the green/yellow conductor of the power cord is joined to this connector the exposed metalwork of the instrument is grounded. The continuity of the protective ground connection must not be broken by the use of 2-core extension cords or 3-prong to 2-prong adapters.

8 Connection of the power cord to the power outlet must be made in accordance with the standard colour code.

	European	American
Line	Brown	Black
Neutral	Blue	White
Ground (Earth)	Green/Yellow	Green

FUNCTIONAL CHECK

9 The check given in paragraph 10 tests the operation of most of the instrument's ciecuits to establish whether the instrument is functioning correctly. The procedure should be followed when the instrument is first taken into use, and after transportation to a new location. It does not check that the instrument is operating to the published specification. Detailed specification tests are given in Section 7 of the maintenance manual.

10 (1) Connect the instrument to a suitable AC supply.

(2) Switch the instrument on. Check that the instrument type-number appears in the display for approximately two seconds, followed by a number which indicates the software version and issue number.

(3) Press the FUNCTION ▼ key until the CHECK indicator lights. Check that the display shows 10.0000000 and that the GATE indicator is flashing.

(4) Press the RESOLUTION ▼ key five times, ensuring that the resolution of the display is decreased by one digit each time.

(5) Press the RESOLUTION ▲ key six times to increase the resolution to nine digits, and check that the GATE TIME indicator shows 1 second.

(6) Press the INPUT A pulse offset key. Check that all LEDs, with the exception of REM, ADDR, SRQ, GATE and STBY/CHRG flash on and off every two seconds. If the GPIB option is installed, the REM, ADDR and SRQ indicators should be lit.

(7) Switch the instrument off.

FREQUENCY STANDARD

11 If it is intended to use an external frequency standard, the frequency standard should be connected to the EXT STD INPUT connector on the rear panel of the instrument. The connection should be made using coaxial cable. Switch on the frequency standard and the instrument: check that the EXT STD indicator on the front panel of the instrument lights.

12 A 10 MHz signal, derived from the frequency standard in use, is available at the 10 MHz STD OUT connector on the rear panel of the instrument. If this signal is used, the connection should be made using coaxial cable.

EXTERNAL ARMING

13 If external arming is to be used, the arming signal should be connected to the EXT ARM INPUT connector on the rear panel.

GATE OUTPUT

14 The gate output is available via probe-hook connectors on the rear panel.

PREPARATION FOR USE WITH THE GPIB

Introduction

15 The instrument must be prepared for use in accordance with the instructions given in Paragraphs 3 to 8 before the instructions given in this section are implemented.

Connection to the GPIB

16 Connection to the GPIB is made via a standard IEEE-488 connector, mounted on the rear panel. The pin assignment is iven in Table 3.1. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

TABLE 3.1

GPIB Connector Pin Assignment

Pin	Signal Line	Pin	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd (6)
7	NRFD	19	Gnd (7)
8	NDAC	20	Gnd (8)
9	IFC	21	Gnd (9)
10	SRQ	22	Gnd (10)
11	ATN	23	Gnd (11)
12	SHIELD	24	Gnd (5 and 17)

Address Setting and Display

17 The interface address is set using five switches, A1 to A5, which are mounted on the rear panel. The permitted address settings, in binary, decimal and ASCII character form, are given in Table 3.2. The GPIB address set can be displayed, in decimal form, by pressing

RECALL LOCAL .

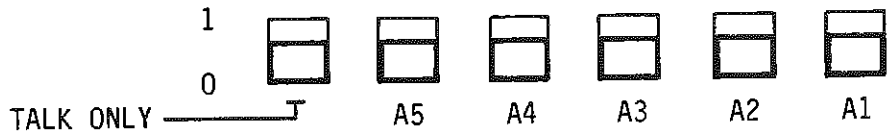
If the address is changed, this key sequence must be repeated to display the new address. The instrument is returned to the measurement mode by pressing

CONTINUE .

18 For addressed operation, the TALK ONLY switch must be in the logic '0' position (down). When this switch is in the logic '1' position, the interface is switched to the talk-only mode. The settings of switches A1 to A5 are then irrelevant.

TABLE 3.2

Address Switch Settings



SWITCH SETTINGS					ADDRESS CODES		
A5	A4	A3	A2	A1	DECIMAL	ASCII LISTEN ADDRESS	ASCII TALK ADDRESS
0	0	0	0	0	0	SP	@
0	0	0	0	1	1	!	A
0	0	0	1	0	2	"	B
0	0	0	1	1	3	#	C
0	0	1	0	0	4		D
0	0	1	0	1	5	%	E
0	0	1	1	0	6	&	F
0	0	1	1	1	7	'	G
0	1	0	0	0	8	(	H
0	1	0	0	1	9	)	I
0	1	0	1	0	10	*	J
0	1	0	1	1	11	+	K
0	1	1	0	0	12	,	L
0	1	1	0	1	13	-	M
0	1	1	1	0	14	.	N
0	1	1	1	1	15	/	O
1	0	0	0	0	16	Ø	P
1	0	0	0	1	17	1	Q
1	0	0	1	0	18	2	R
1	0	0	1	1	19	3	S
1	0	1	0	0	20	4	T
1	0	1	0	1	21	5	U
1	0	1	1	0	22	6	V
1	0	1	1	1	23	7	W
1	1	0	0	0	24	8	X
1	1	0	0	1	25	9	Y
1	1	0	1	0	26	:	Z
1	1	0	1	1	27	;	[
1	1	1	0	0	28	<	/
1	1	1	0	1	29	=	]
1	1	1	1	0	30	>	^

GPIB CHECK

19 The procedure which follows checks the ability of the instrument to accept, process and send GPIB messages. The correct functioning of the instrument under local control should be verified before the procedure is attempted.

20 The recommended test equipment is the Hewlett-Packard HP-85 GPIB controller, with the I/O ROM in the drawer. It is assumed that the select code of the controller I/O port is 7, and that the address of the instrument is 16 (to change the address see Paragraph 17). If any other controller or select code/address combination is used, the GPIB commands given in the following paragraphs will require modification. The controller should be connected to the GPIB interface of the instrument via a GPIB cable. No connection should be made to the channel A or B inputs, or to the D input.

21 Successful completion of the GPIB check proves that the instrument's GPIB interface is operating correctly. The procedure does not check that all the device-dependent commands can be executed. However, if the GPIB interface works correctly and the instrument operates correctly under local control, there is a high probability that it will respond to all device-dependent commands.

Remote and Local Message Check

22 Switch the instrument on. Check that the REM, ADDR and SRQ indicators flash on and off once. If the indicators do not flash, or if they flash continuously, there is a fault on the GPIB board.

23 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 716	

Check that the REM indicator lights.

24 Test as follows:

Action	HP-85 Code	Your Controller
Send the device-dependent command CK	OUTPUT 716; "CK"	

Check that the ADDR indicator lights and that the Check mode is selected.

25 Test as follows:

Action	HP-85 Code	Your Controller
Send the instrument's listen address followed by the GTL message	LOCAL 716	

Check that the REM indicator is off. The ADDR indicator will also be off if the controller used sends the unlisten message (UNL) true automatically. This is the case when using the HP-85.

Local Lockout and Clear Lockout Check

26 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 716	
Send the LLO message	LOCAL LOCKOUT 7	

Check that the REM indicator lights. Operate the LOCAL key on the front panel and verify that the REM indicator remains lit.

27 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message false	LOCAL 7	

Check that the REM indicator is off.

28 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true, together with the instrument's listen address	REMOTE 716	

Check that the REM indicator lights. Press the LOCAL key and verify that the REM indicator turns off.

Data Output Check

29 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the check mode by sending the listen address, followed by the device-dependent command CK	OUTPUT 716; "CK"	
Prepare a store to receive a 21-byte data string	DIM Z$ [21]	
Send the instrument's talk address. Store the 21-byte data string in the prepared store	ENTER 716; Z$	
Display the contents of the store	DISP Z$	

Check that the display reads CK+0010.0000000E+06 with the cursor moved to the next line, indicating that carriage return (CR) and line feed (LF) have been accepted.

SRQ and Status Byte Check

30 Test as follows:

Action	HP-85 Code	Your Controller
Send the REN message true	REMOTE 7	
Set the instrument to send the SRQ message when an error is detected, and force the generation of error code 05 by sending the device-dependent command XXX	OUTPUT 716;"IPXXX"	
Store the status of the GPIB interface of the controller, in binary form, as variable T	STATUS 7, 2; T	
Display the status of the SRQ line	DISP"SRQ=";BIT(T,5)	

Check that the HP-85 displays SRQ=1, the SRQ status bit is at logic '1' or the SRQ line is $\leq$0.8 V. Check that the SRQ indicator on the instrument is lit.

31 Test as follows:

Action	HP-85 Code	Your Controller
Conduct a serial poll and store the status byte as variable R	R = SPOLL (716)	
Display variable R	DISP "R="; R	

Check that the SRQ indicator is turn off when the serial poll is made. The value of R shoud be 101 (in binary form, R should be 0000000001100101). If using an HP-85 controller, check that the ADDR indicator is turned off.

Device Clear and Selected Device Clear Check

32 Test as follows:

Action	HP-85 Code	Your Controller
Set the instrument to the FREQ B mode by sending the listen address, followed by the device-dependent command FB	OUTPUT 716;"FB"	
Send the DCL message true	CLEAR 7	

Check that the function indicated on the instrument front panel changes to FREQ A.

33 Test as follows:

Action	HP-85 Code	Your Controller
Reset the instrument to the FREQ. B mode by sending the listen address, followed by the device-dependent command FB	OUTPUT 716;"FB"	
Send the SDC message true	CLEAR 716	

Check that the function indicated on the instrument front panel changes to FREQ A.

IFC Check

34 Test as follows:

Action	HP-85 Code	Your Controller
Send the ATN message false Send the IFC message true	RESUME 7 ABORTIO 7	

Check that the ADDR indicator is turned off.

TALK ONLY Selector Test

35 (1) Set the TALK ONLY switch in the instrument rear panel to '1'. Check that the REMOTE indicator is turned off and the ADDR indicator lights.

(2) Set the TALK ONLY switch to '0'. Check that the ADDR indicator is turned off.

OPTION FITTING INSTRUCTIONS

Single-Instrument Fixed Rack Mounting Kit 11-1648 (Option 60A)

36 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	1	16-0643
Long mounting bracket	1	16-0644
Screw, M4 x 16	4	24-7733
Crinkle washer M4	4	24-2802
Spacer, plain M4 x 5	4	24-4112
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

37 Assemble the kit to the instrument as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument s feet from the bottom cover.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) At one side of the instrument, secure a mounting bracket to the side frame, using two spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(8) Repeat step (7) at the other side of the instrument.

(9) Fit the cup washers to the M6 screws. Offer the instrument up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts.

Double-Instrument Fixed Rack Mounting Kit 11-1649 (Option 60B)

38 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	2	16-0643
Screw, M4 x 16	4	24-7733
Crinkle washer, M4	4	24-2802
Spacer, plain, M4 x 5	4	24-4112
Spacer, female	2	14-1583
Spacer, male	2	14-1584
Mating plate	1	13-2000
Rivet, plastic	4	24-3211
Screw, M6 x 16	4	24-7995
Cup washer, M6	4	24-2809
Caged nut, M6	4	24-2240

39 Prepare both instruments as follows:

(1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the bottom cover by sliding it towards the rear of the instrument.

(4) Remove the instrument's feet from the bottom cover.

(5) Replace the bottom cover. Replace and secure the bezel.

(6) Remove the four blind grommets from the sides of the instrument. This will reveal two threaded holes in each side frame.

(7) Remove two buffers from the bezel at the side which is to be at the centre of the rack.

40 Assemble the kit to the instruments as follows:

(1) At the sides which are to be at the centre of the rack, secure the female spacers to one instrument and the male spacers to the other. The spacers screw into the threaded holes in the side frames.

(2) At the other side of each instrument, secure a mounting bracket to the side frame, using two plain spacers, M4 screws and crinkle washers. Position the spacers between the mounting bracket and the side frame.

(3) Fit the male spacers on one instrument into the female spacers on the other.

(4) Position the mating plate to bridge the gap between the bezels. Secure it by pushing the plastic rivets through the plate into the buffer holes.

(5) Fit the cup washers to the M6 screws. Offer the two instruments up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts.

PCB-Mounted Frequency Standard, 11-1713 (Option 04T)

41 The kit comprises:

Item	Qty	Racal-Dana Part Number
Plate assembly	1	11-1610
Oscillator PCB	1	19-1208
Crinkle washer M3	3	24-2801
Screw, M3 x 6	3	24-7721

Installation

42 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard already fitted. Instructions are given in Paragraph 43 or Paragraph 46, according to type.

(5) Secure the PCB to the plate assembly, using an M3 screw and washer from the kit. The screw should be passed through the mounting hole in the board and screwed into the threaded spacer of the plate assembly. The component side of the board should be towards the plate assembly.

(6) Connect the PCB to the motherboard at PL14, with the plate assembly towards the rear panel of the instrument.

(7) Secure the plate assembly to the rear panel, using two M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the plate assembly.

(8) Replace the top cover. Replace and secure the bezel.

Removal

43 (1) Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel.

(2) Pull the PCB and plate assembly upwards until the board is disconnected from the motherboard.

Ovened Frequency Standards 11-1710 and 11-1711 (Options 04A and 04B)

44 The kit comprises:

Item	Qty	Racal-Dana Part Number
Oscillator assembly	1	9444 for 11-1710 9423 for 11-1711
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

Installation

45 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard already fitted. Instructions are given in Paragraph 43 or Paragraph 46, according to type.

(5) Connect the flying lead on the oscillator assembly to SK14 on the motherboard.

(6) Secure the oscillator assembly to the rear panel of the instrument, using the M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the oscillator assembly.

(7) Replace the top cover. Replace and secure the bezel.

Removal

46 (1) Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel.

(2) Lift the oscillator assembly out of the chassis and disconnect the flying lead from the motherboard at PL14.

Reference Frequency Multiplier Option 11-1645 (Option 10)

47 The kit comprises:

Item	Qty	Racal-Dana Part Number
Frequency multiplier	1	19-1164
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

48 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the frequency standard if an ovened type is fitted.

(5) Remove the shorting links from between pins 5 and 6 and pins 8 and 9 on PL16.

NOTE:
These links should be stored in a safe place. They must be replaced if Option 10 is removed from the instrument.

(6) Connect the frequency multiplier PCB to the motherboard at PL16 and PL17, with the threaded spacers towards the right-hand side frame.

(7) Secure the PCB to the side frame, using the M3 screws and washers.

(8) Replace and secure the frequency standard if it was removed in (5).

(9) Replace the top cover. Replace and secure the bezel.

GPIB Option 11-1724 (Option 55)

49 The kit comprises:

Item	Qty	Racal-Dana Part Number
GPIB board assembly	1	19-1146
Bracket	2	11-1728
Speednut	2	24-0146
Shakeproof washer, M3	2	24-2813
Screw, M3 x 6	3	24-7721
Washer Plain M3	1	24-2703
Washer Crinkle M3	1	24-2801
Screw, M4 x 10 C'SK	4	24-7543
Washer Nylon	4	24-2816

NOTE 1:
This option cannot be fitted to an instrument aleady fitted with the battery pack option.

NOTE 2: (1999 only)
One speednut, bracket and fixing screw are not required for this instrument and should be discarded.

50 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument.

(5) Slide a speednut onto a bracket. Ensure that the flat non-threaded face of the speednut is uppermost.

(6) (a) Secure a bracket to LH sideframe of the instrument using the M4 screws and nylon washers supplied.

(b) 1998 only: secure a bracket to RH sideframe of the instrument using the M4 screws and nylon washers supplied. Ignore the two holes near the rear of the instrument.

(7) Hold the GPIB board, component side down, with the GPIB connector towards the rear panel. Connect the ribbon-cable to the motherboard at SK4.

(8) Tilt the GPIB board, and lower it into the instrument, easing the GPIB connector into the shaped cut-out in the rear panel of the instrument.

(9) (a) 1998 only: line-up the holes in the GPIB board with the speednuts (move the speednuts slightly if necessary). Insert the two self-tapping screws through the board into the speednuts. Do not tighten screws.

(b) 1999 only: line-up the hole and slot in the GPIB board with the speednut and threaded hole in the prescaler screen (move the speednut slightly if necessary). Insert, through the board, the self-tapping screw into the speednut and the M3 screw with crinkle and plain washers into the threaded hole, in the prescaler screen. Do not tighten screws.

(10) Secure the bracket which carries the GPIB connector to the rear panel, using the two M3 screws and shakeproof washers. Tighten screws.

NOTE:
The screws and washers provide the ground connection between the GPIB connector and the instrument chassis. Tighten the screws firmly to ensure that a good connection is obtained.

(11) Tighten screws in Para 50, 9(a) or 9(b).

(12) Replace the top cover. Replace and secure the bezel.

Battery Pack Option 11-1625 (Option 07)

51 The kit comprises:

Item	Qty	Racal-Dana Part Number
PCB assembly	1	11-1722
Mounting bracket	1	11-1599
Battery pack	1	11-1723
Cover plate	1	13-2040
Crinkle washers, M3	5	24-2801
Screws, M3 x 6	5	24-7721
Crinkle washers, M4	2	24-2802
Screws, M4 x 8	2	24-7730
Plain washers, M4	2	24-2705
Spare fuse, 3A	1	24-0069
Plastic rivet	1	24-0252
Washer, nylon	4	24-2816
Screw, M4 x 10 C'SK	4	24-7543
Plain washer M3	3	24-2703

NOTE 1:
This option cannot be fitted to an instrument already fitted with the GPIB interface option.

NOTE 2:
1999 only: the RH mounting bracket with some screws and washers included in the kit are not required for this instrument and should be discarded.

52 (1) Disconnect the AC power cord at the rear panel.

(2) Remove the two screws which secure the bezel to the rear panel: remove the bezel.

(3) Remove the top cover by sliding it towards the rear of the instrument.

(4) Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument.

(5) If a PCB-mounted frequency standard is fitted, remove the two screws adjacent to the FREQ STD ADJUST aperture.

(6) Remove the four screws which secure the rear panel to the side frames.

(7) Ease the rear panel away from the instrument until it disconnects from the motherboard at PL19 and PL20.

(8) Hold the PCB assembly with the switches towards the rear of the instrument and the PCB connector pointing downwards.

(9) Lower the assembly into the chassis and connect the PCB to the motherboard at PL21, taking care that it mates correctly.

(10) Replace and secure the rear panel.

(11) If a PCB-mounted frequency standard is fitted, secure it to the rear panel with the screws removed in (5).

(12) Position the cover plate over the switches protruding through the rear panel. Secure the cover plate and the rear panel to the PCB assembly, using the M3 screws and crinkle washers.

(13) 1998 only: Secure the mounting bracket to the right-hand side frame, using two M4 screws and crinkle washers. The horizontal flange should be towards the top of the instrument.

(14) Position the battery pack within the chassis with the flying lead towards the rear of the instrument and the supporting lugs resting on the mounting bracket for the 1998 or prescaler screen for the 1999. Secure the battery pack to the left-hand side frame, using, for the 1998, two M4 screws, two crinkle washers and the plastic rivet. For the 1999 use the two M4 C'SK screws, two nylon washers and the plastic rivet.

(15) Secure the supporting lugs to the mounting bracket (1998) using M4 screws, plain and crinkle washers or to the prescaler screen (1999), using M3 screws, plain and crinkle washers.

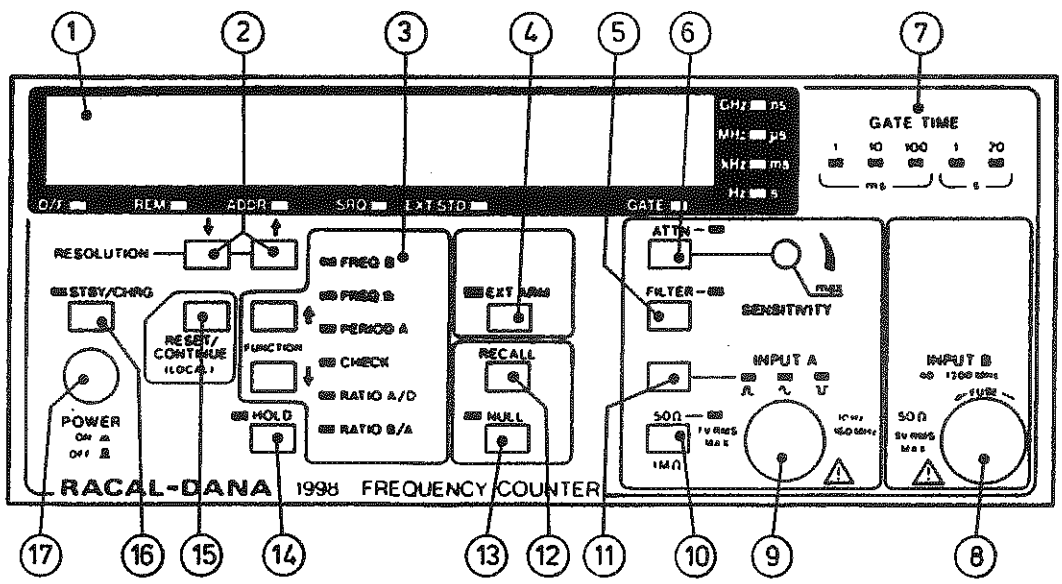
(16) Connect the flying lead on the battery pack to the connector on the PCB assembly.

(17) Replace the top cover. Replace and secure the bezel.

SECTION 4 OPERATING INSTRUCTIONS

INTRODUCTION

1 The instrument should be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC voltage selector.



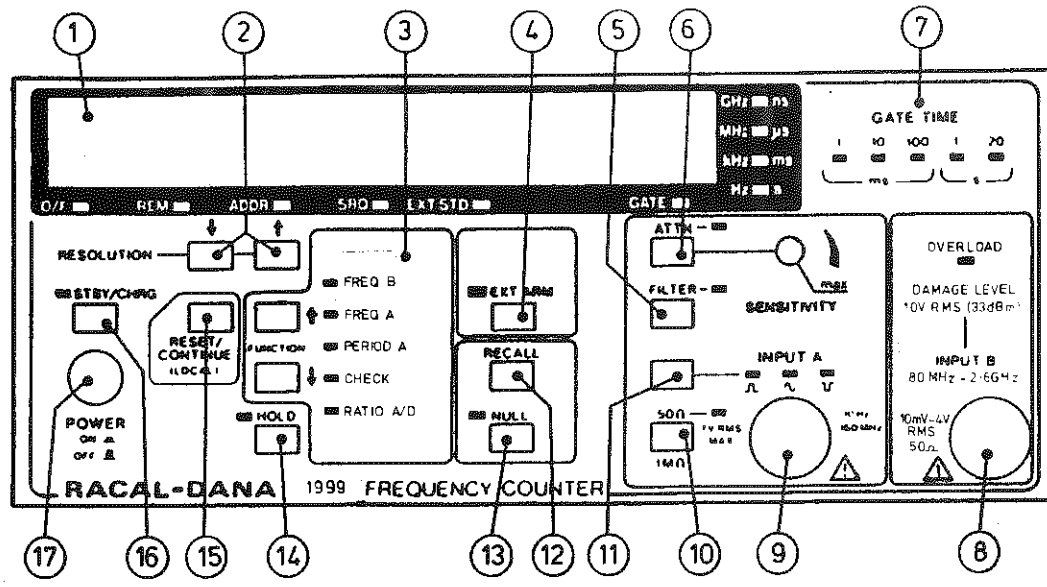
DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS

Front Panel Items

2

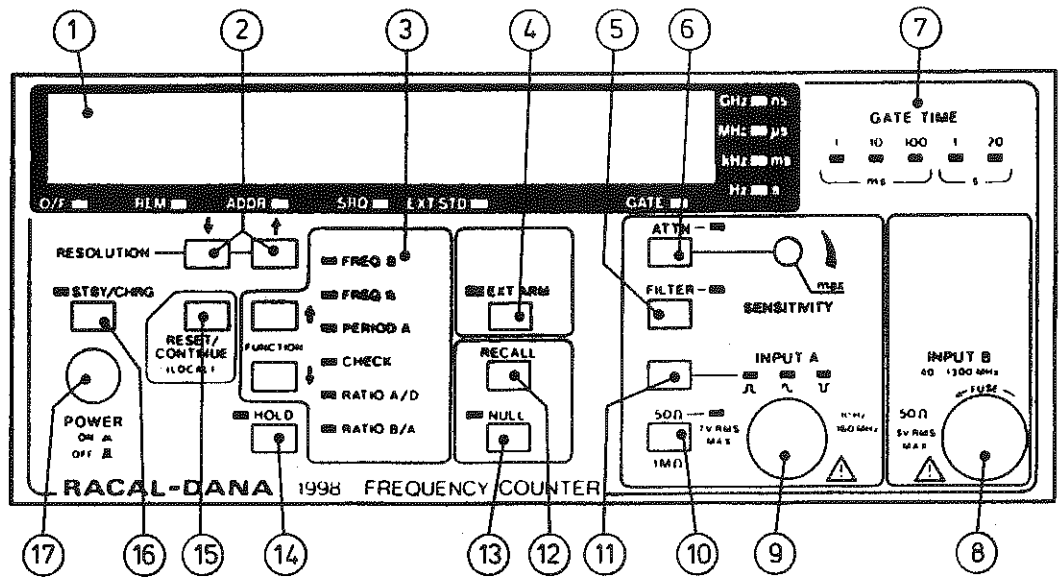
Reference	Item	Description
①	Display	A 10-digit LED display, used to display (1) The result of a measurement (2) A number recalled from an internal store. (3) Error indications.

Reference	Item	Description
	O/F Indicator	Lights when the measurement result has overflowed the most significant digit of the display.
	REM Indicator	Lights when the instrument is operating under remote control.
	ADDR Indicator	Lights when the instrument is acting as a listener or as a talker.
	SRQ Indicator	Lights when the instrument generates a service request.
	EXT STD Indicator	Lights when the instrument is operating from an external frequency standard.
	GATE Indicator	Lights while a measurement cycle is in progress.
	Display Units Indicators	Four indicators show the scale of the display in terms of frequency or time period.
②	Resolution Control Keys	Used to step the display resolution up or down as shown by the arrows
③	Function Selector	The functions can be selected in turn using the FUNCTION ↑ and ↓ keys. The function selection 'wraps round' at both ends.
④	EXT ARM Key and Indicator	Used to enable and disable the external start arming. The indicator lights when the external arming facility is selected.
⑤	FILTER Key	Successive operations enable and disable the channel A input filter. The indicator lights when the filter is enabled.
⑥	ATTN and SENSITIVITY controls and indicator	ATTN selects x1 or x20 input signal attenuation. The indicator lights when x20 attenuation is selected. The sensitivity can be continuously adjusted over a range of approximately 58 dB by means of the SENSITIVITY control and the x20 attenuator.



Reference	Item	Description
⑦	GATE TIME Indicators	These show the gate time as set by the selected resolution.
⑧	INPUT B Connector (1998) INPUT B Connector (1999) and O/load Indicator	BNC fused connector for inputs from 40 MHz to 1.3 GHz. N type connector for inputs from 80 MHz to 2.6 GHz. Overload indicator lights when B input signal exceeds 4.8 V ± 0.8 V. NOTE: Due to hysterisis, the input signal overload indicator will only be extinguished by substantially reducing the input signal voltage level.
⑨	INPUT A Connector	BNC connector for inputs from 10 Hz to 160 MHz.
⑩	50 Ω/1 MΩ Key	Used to select 50 Ω or 1 MΩ input impedance. The indicator lights when 50 Ω is selected.
⑪	INPUT A pulse offset key	Used to select the trigger level according to the mark/space ratio of the input waveform. The indicators show the mark/space ratio range: ⎍ low (less than 1:2.5) ∿ medium (1:2.5 to 2.5:1) ⎍ high (more than 2.5:1) The key selects each in turn at successive presses.

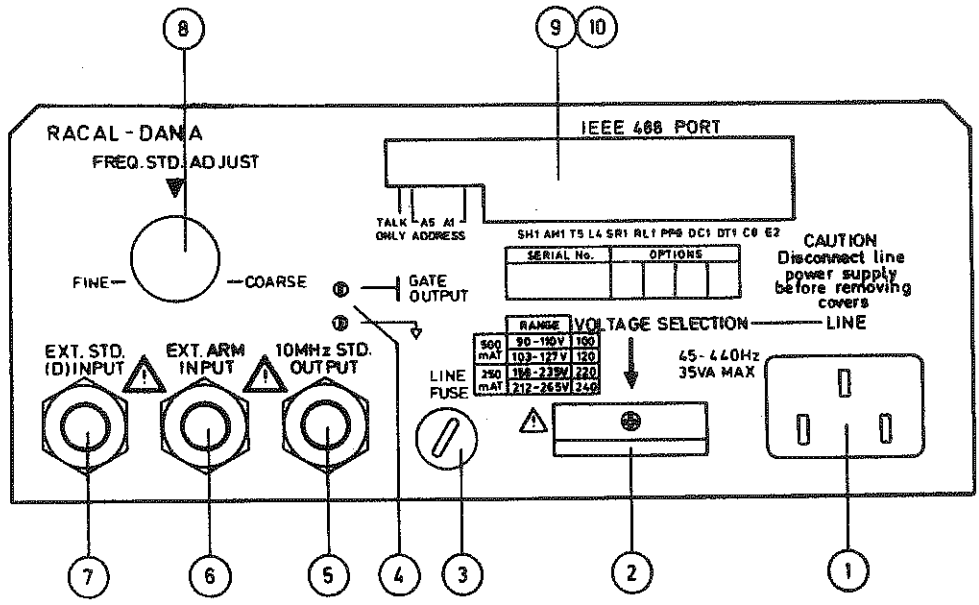
Reference	Item	Description
⑫	RECALL Key	Used in conjunction with NULL and RESET keys. [RECALL] [NULL] displays the value in the null store. [RECALL] [RESET] displays the GPIB address when this option is fitted.
⑬	NULL Key and Indicator	Key enables and disables the NULL function. At the time that the NULL function is enabled the currently-displayed value is stored in the null register. The indicator lights when NULL is selected.
⑭	HOLD Key and Indicator	Successive operations put the instrument into and out of the Hold (single-shot measurement) mode. The indicator lights when the instrument is in the Hold mode. Readings are triggered using the RESET key.
⑮	RESET/CONTINUE (LOCAL) Key	This key has three functions. RESET Clears the display and triggers a new measurement cycle when the instrument is in the measurement mode. CONTINUE Returns the instrument to the measurement mode and triggers a measurement cycle. It can also be used to clear the OP Er indication. LOCAL Returns the instrument to local control from remote GPIB control provided local lockout is not set.



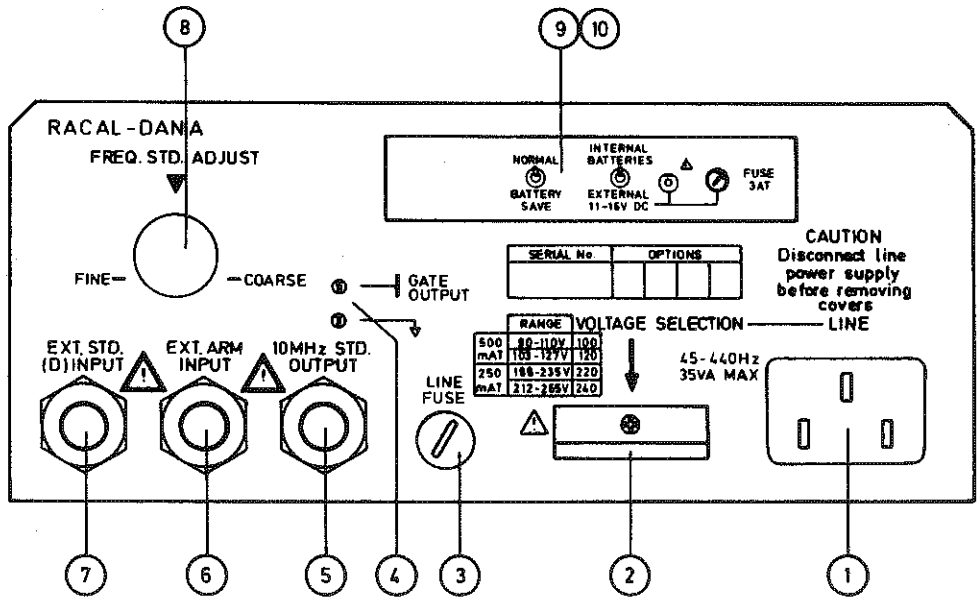
Reference	Item	Description
(16)	STBY/CHRG Key and Indicator	Successive operations switch the instrument into and out of the standby state. The indicator lights when the instrument is in the standby state. If the battery pack option is installed the indicator flashes when the battery approaches the discharged state. The battery is charged at the full rate when the instrument is in standby and external power is applied.
(17)	POWER Switch	Controls the AC or DC power to the instrument.

3 **Rear Panel Items**

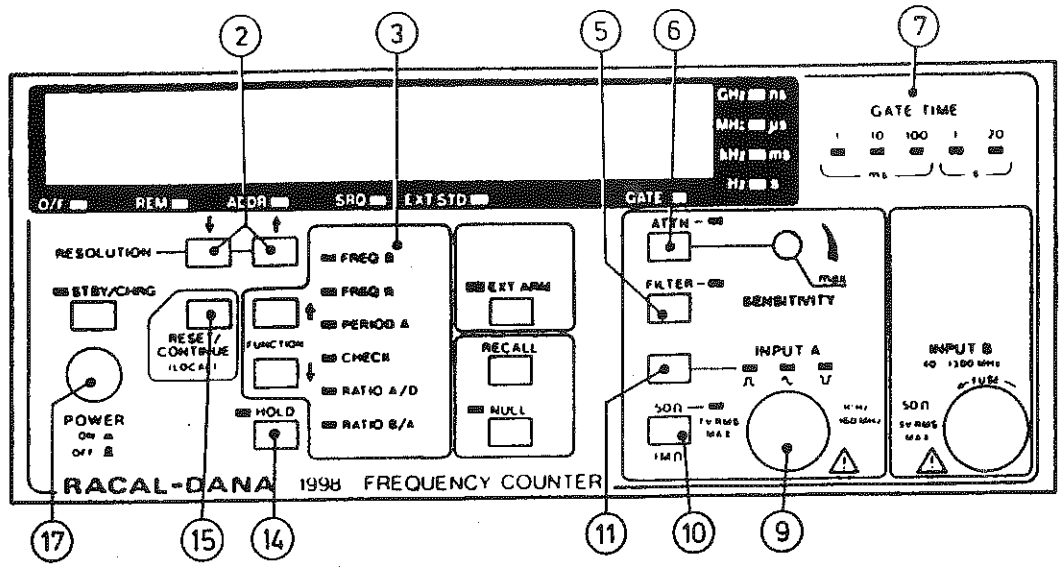
Reference	Item	Description
①	AC Power Input Plug	A standard connector for the AC power supply. A RFI filter is incorporated.
②	Line Voltage Selector	Voltage selection is changed by repositioning a printed circuit board. The voltage selected can be seen through a window in the retaining clamp of the card.
③	Line Fuse	A ¼ in x 1¼ in, surge-resistant, glass cartridge fuse. The required fuse ratings for different line voltage ranges are shown on the panel and in Section 3 of this manual.
④	GATE OUTPUT	The gate output is available at a pair of tags for use with hook probes. The gate waveform is delayed by 10 nsec typically (15 nsec maximum).
⑤	10 MHz STD OUTPUT	A BNC connector, providing a 10 MHz signal locked to the frequency standard in use.
⑥	EXT ARM INPUT	A BNC connector for accepting external arming signals.
⑦	EXT STD (D) INPUT	A BNC connector for connecting an external frequency standard input. The frequency required is 10 MHz unless the reference frequency multiplier option is fitted. With this option, frequencies of 1 MHz, 2 MHz, 5 MHz and 10 MHz are acceptable. This connector is also used as the signal input for channel D.
⑧	FREQ. STD. ADJUST	This aperture provides access to allow adjustment of the internal frequency standard.



Reference	Item	Description
(9)	GPIB Option	
	GPIB Address Switches	Switches A1 to A4 define the listen and talk addresses for GPIB operation in the addressed mode. The talk-only switch must be in the 'Ø' position. With the talk-only switch in the '1' position the instrument is set to the talk-only condition. The positions of switches A1 to A5 are then irrelevant.
	GPIB Connector	An IEEE-488-1978 standard connector used to connect the instrument to the GPIB. An adapter, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an accessory.



Reference	Item	Description
(10)	Battery-pack Option	
	External DC Input	Permits the instrument power to be derived from an external fused DC supply.
	Battery NORMAL/SAVE Switch	Used to select the Battery-Save facility.
	INTERNAL/EXTERNAL DC Supply Switch	Used to select operation from the internal battery or an external DC supply.
	DC Supply Fuse	A ¼ in x 1¼ in glass cartridge fuse of the surge-resistant type. The required rating is 3 AT.



FREQUENCY MEASUREMENT - INPUT A

4 This facility measures either sinewave or pulse-train. For measuring bursts of signal refer also to Paragraph 9.

(1) Press the POWER switch (17) to switch on.

(2) Select FREQ A, using the FUNCTION keys (3) .

(3) Select the required input impedance (10) and attenuation (6) .

(4) Select the trigger level (11) according to the mark/space ratio of the input waveform.

(5) Select the required display resolution, using the RESOLUTION keys (2) . Note that the gate time is related to the resolution. One of the GATE TIME indicators (7) will show the gate time.

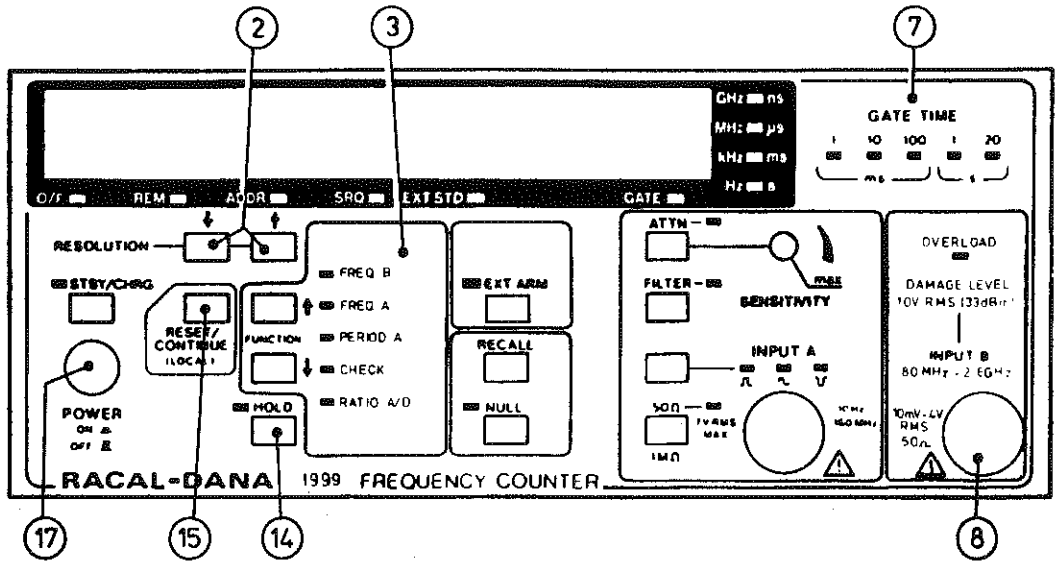
(6) If a frequency below 50 kHz is to be measured in the presence of HF noise, select the low-pass input filter (5) .

(7) Connect the signal to be measured to INPUT A (9) .

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(8) Adjust the SENSITIVITY control (6) for a stable reading (can usually be left at MAX).

(9) If hold mode operation is required, select HOLD (14) . To take a measurement, press the RESET key (15) . Check that the GATE indicator lights during the measurement period. To retun to the continuous measurement mode, press the HOLD key (14) again.



FREQUENCY MEASUREMENT - INPUT B

5 This faciity measures either sinewave or pulse-train. For measuring bursts of signal, refer also to Paragraph 9.

(1) Press the POWER switch (17) to switch on.

(2) Select FREQ B, using the FUNCTION keys (3) .

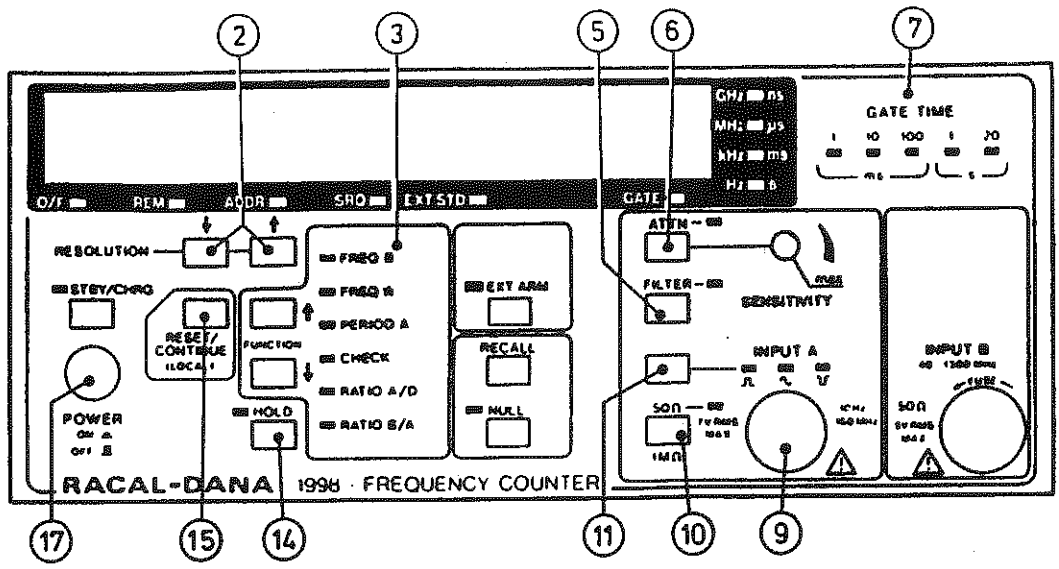
(3) Connect the signal to be measured to INPUT B (8) .

(4) Ensure overload LED is not lit. (1999 ONLY).

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT SIGNAL LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(5) Select the required display resolution, using the RESOLUTION keys (2) . Note that the gate time is related to the resolution. One of the GATE TIME indicators (7) will show the gate time.

(6) If hold mode operation is required, select HOLD (14) . To take a measurement, press the RESET key (15) . Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (14) again.



PERIOD MEASUREMENT

6 This facility measures the period of either sinewave or pulse-train signals. For period measurements on bursts of signal, refer also to Paragraph 9.

(1) Press the POWER switch (17) to switch on.

(2) Select PERIOD A, using the FUNCTION keys (3) .

(3) Select the required input impedance (10) and attenuation (6) .

(4) Select the trigger level 11 according to the mark/space ratio of the input waveform.

(5) Select the required display resolution, using the RESOLUTION keys (2) . Note that the gate time is related to the resolution. One of the GATE TIME indicators (7) will show the nominal gate time.

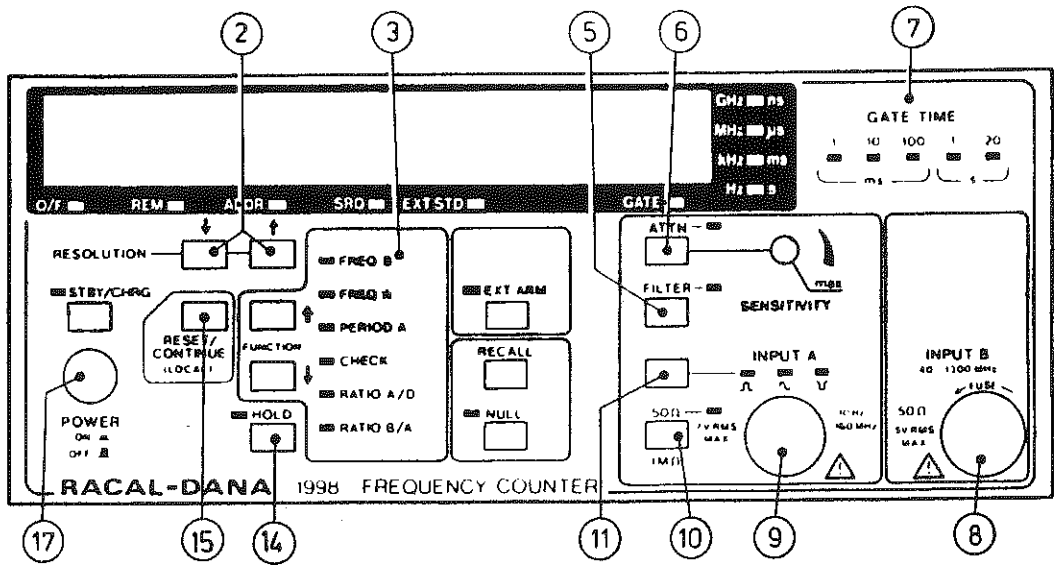
(6) If a frequency below 50 kHz is to be measured in the presence of HF noise, select the low-pass input filter (5) .

(7) Connect the signal to be measured to INPUT A (9) .

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(8) Adjust the SENSITIVITY control (6) for a stable reading (can usually be left at MAX).

(9) If hold mode operation is required, select HOLD (14) . To take a measurement, press the RESET key (15) . Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (14) .



RATIO MEASUREMENT B/A (1998 only)

7 This facility measures the frequency ratio of the signals at INPUT B and INPUT A. It provides, for example, an easy way of setting an adjustable signal source to match that of a fixed source of an awkward value - simply adjust for a reading of 1.0.

(1) Press the POWER switch (17) to switch on.

(2) Select RATIO B/A, using the FUNCTION keys (3) .

(3) Select the required A channel input impedance 10 and attenuation (6) .

(4) Select the trigger level (11) according to the mark/space ratio of the input waveform.

(5) If a frequency of the A channel input is known to be below 50 kHz, and is in the presence of HF noise, select the low-pass input filter (5) .

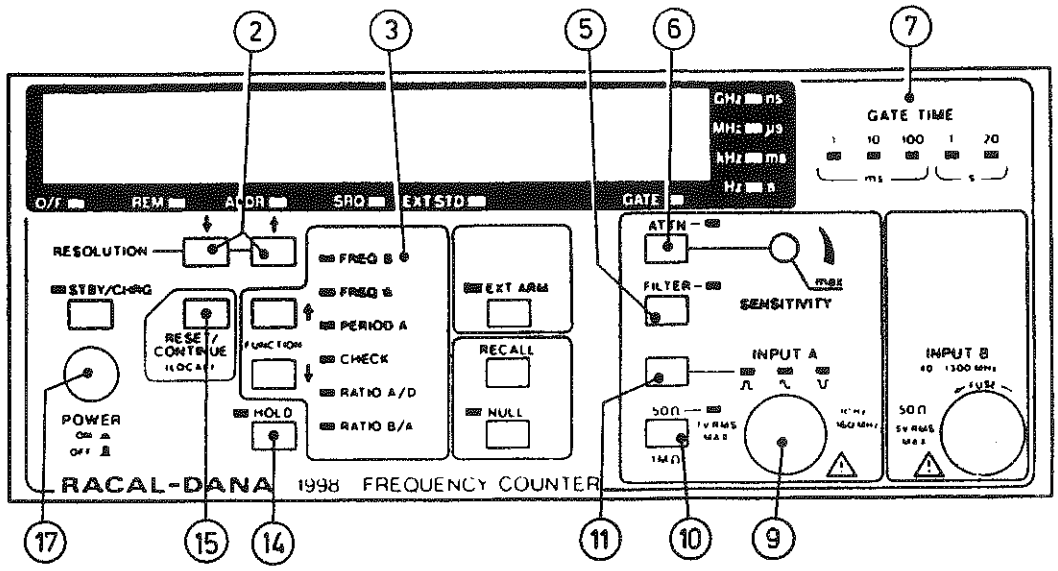
(6) Connect the lower-frequency signal to INPUT A (9) , and the higher-frequency signal to INPUT B (8) .

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(7) Adjust the SENSITIVITY control (6) for a stable reading (can usually be left at MAX).

(8) Select the required display resolution, using the RESOLUTION keys (2) . Note that the gate time is related to the resolution. One of the GATE TIME indicators (7) will show the nominal gate time.

(9) If hold mode operation is required, select HOLD (14) . To take a measurement, press the RESET key (15) . Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (14) .



RATIO MEASUREMENT A/D

8 This facility measures the frequency ratio of the signals at INPUT A and the EXT. SD. (D) INPUT connector on the rear panel.

(1) Press the POWER switch (17) to switch on

(2) Select RATIO A/D, using the FUNCTION keys (3) .

(3) Select the required A channel input impedance (10) and attenuation (6) .

(4) Select the trigger level (11) according to the mark/space ratio of the input waveform.

(5) If a frequency below 50 kHz is to be measured in the presence of HF noise, select the low-pass input filter (5) .

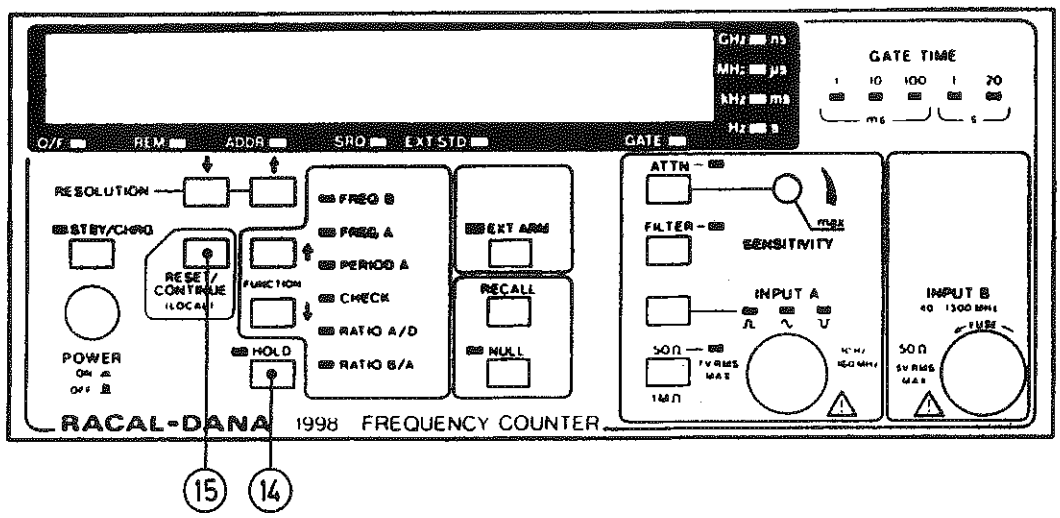
(6) Connect the higher-frequency signal to INPUT A (9) , and the lower-frequency input signal to the rear-panel EXT. STD. (D) INPUT connector.

CAUTION: SIGNAL LEVEL
ENSURE THAT THE INPUT LEVEL DOES NOT EXCEED THE DAMAGE LEVELS SPECIFIED IN SECTION 1 OF THIS MANUAL.

(7) Adjust the SENSITIVITY control (6) for a stable reading (can usually be left at MAX).

(8) Select the required display resolution, using the RESOLUTION keys (2) . Note that the gate time is related to the resolution. One of the GATE TIME indicators (7) will show the nominal gate time.

(9) If hold mode operation is required, select HOLD (14) . To take a measurement, press the RESET key (15) . Check that the GATE indicator lights during the measurement period. To return to the continuous measurement mode, press the HOLD key (14) .



SIGNAL BURST (SINGLE-SHOT) MEASUREMENT

9 This facility is for measuring individual burst of signals, either sinewave or pulse-train.

(1) Set the instrument up for normal measurements, as described in Paragraphs 4 to 8.

(2) Ensure that the displayed gate time selected is at least 1 msec shorter than the signal burst to be measured.

(3) Press the HOLD key (14) . If there is an existing reading on the display, this will be held.

(4) Press the RESET key (15) to clear the instrument's registers and prime the circuits ready for the input signal burst. The measurement will be preceded by a 1 ms delay to allow for the input signal settling time, and is initiated upon receipt of the input signal.

(5) Check that the GATE indicator lights during the measurement period.

(6) The reading is held until either a new measurement is primed by pressing RESET, or the HOLD key is pressed again to return the instrument to the continuous measurement mode.

NULL FACILITY

10 The null facility allows a displayed value to be entered into the internal NULL store. When the null facility is enabled (NULL indicator lit) the display indicates

(measured value minus the value held in the NULL store).

11 The null facility is available with the frequency, period and ratio functions.

12 (1) If nulling from the present measured value use the procedures given in Paragaphs 4 to 8 to make the instrument display the required value. If nulling from a value already in the NULL store, press

[RECALL] [NULL] .

The value in the NULL store will be displayed.

(2) To enable the NULL facility, press

[NULL] .

The NULL indicator will light. The displayed value will be entered into the NULL store. When a new measurement is made the display indicates the difference between the measured value and the value in the NULL store.

(3) To disable the null facility, press

[NULL] .

The NULL indicator will go out and the display will indicate the measured value. The value in the NULL store is unchanged.

13 The value held in the NULL store can be displayed at any time by pressing

[RECALL] [NULL] .

To return the instrument to the status existing before the NULL store contents were displayed press

[CONTINUE] .

EXTERNAL ARMING

14 External arming allows a measurement to be started at a particular time, so allowing measurements to be made on predetermined parts of the input waveform (such as a particular tone burst in a tone-burst sequence).

15 The start circuit is armed by a positive-going edge of the external arming signal. The gate will be opened by the signal to be measured. The gate time is set by the RESOLUTION controls. A new measurement cycle will be re-armed by the first external arming pulse received after the internal gate is closed and computation is completed. External arming pulses occurring while the gate is open are ignored.

16 External arming may also be used in conjunction with the hold facility. A single measurement will be made and held on the display following the receipt of an external arming pulse. Further arming pulses will be ignored until the RESET key is pressed. A new measurement cycle will then be started by the next arming pulse received.

17 External arming is enabled and disabled by pressing the EXT ARM key. The indicator lights when external arming is enabled.

18 The external arming signal is connected to the EXT ARM INPUT socket on the rear panel. The pulse must have a minimum duration of 200 ns. There is a delay of not more than 100 ns between the positive-going edge of the arming pulse and the completion of arming.

DISPLAY RESOLUTION

19 Resolution refers to the number of zeros displayed when no signal is applied at the input. The resolution can be set to display from 3 to 10 decimal places. A 10% overrange of the display is permitted without a change of range. Because of this, an additional digit with a value of 1 may appear at the more significant end of the display when measurements are made. With a resolution of 10 selected, the presence of this extra digit is shown by the overflow indicator.

20 When ratio measurements are made, no more than seven digits (plus a possible overrange digit) are displayed, regardless of the resolution selected.

21 The resolution is changed using the step-up ↑ and step-down ↓ keys. To step up from nine to ten digits, the step-up key must be held down for about two seconds.

GATE TIME

22 Gate time is related to the resolution selected, as shown in Table 4.1.

TABLE 4.1

Resolution and Gate Time

Resolution	Gate Time
10	20 s
9	1 s
8	100 ms (see NOTE 2)
7	10 ms
6	1 ms
5	1 ms ┐
4	1 ms ├ (see NOTE 3)
3	1 ms ┘

NOTE 1:
The gate times shown are nominal. Due to the use of the recipromatic counting technique the gate time may be extended by:

(1) Up to two periods of the input signal on FREQ A and PERIOD A.

(2) Up to 64 (for 1998); 256 (for 1999) periods of the input signal on FREQ B.

(3) Up to one period of the input signal on channel A when measuring RATIO B/A (1998 only) or RATIO A/D.

NOTE 2:
A resolution of 8 is selected when the instrument is first switched on.

NOTE 3:
With resolutions of 3, 4 and 5 selected, measurements are averaged.

GATE OUTPUT SIGNAL

23 The internally generated gate waveform is available at the GATE OUTPUT connectors on the rear panel. The waveform is delayed by not more than 15 ns relative to the true measurement period.

24 This waveform can be used, together with external arming, to assist in selecting a single tone burst from a tone burst sequence. Displaying the signal to be measured and the gate waveform on an oscilloscope allows the external arming pulse to be delayed until the gate time falls within the specific burst of interest.

25 When the instrument is operating in the hold mode, the gate waveform is preceded by a 100 µs prepulse and a hold-off period of approximately 1 ms.

26 Typical gate waveforms are shown in Fig 4.1.

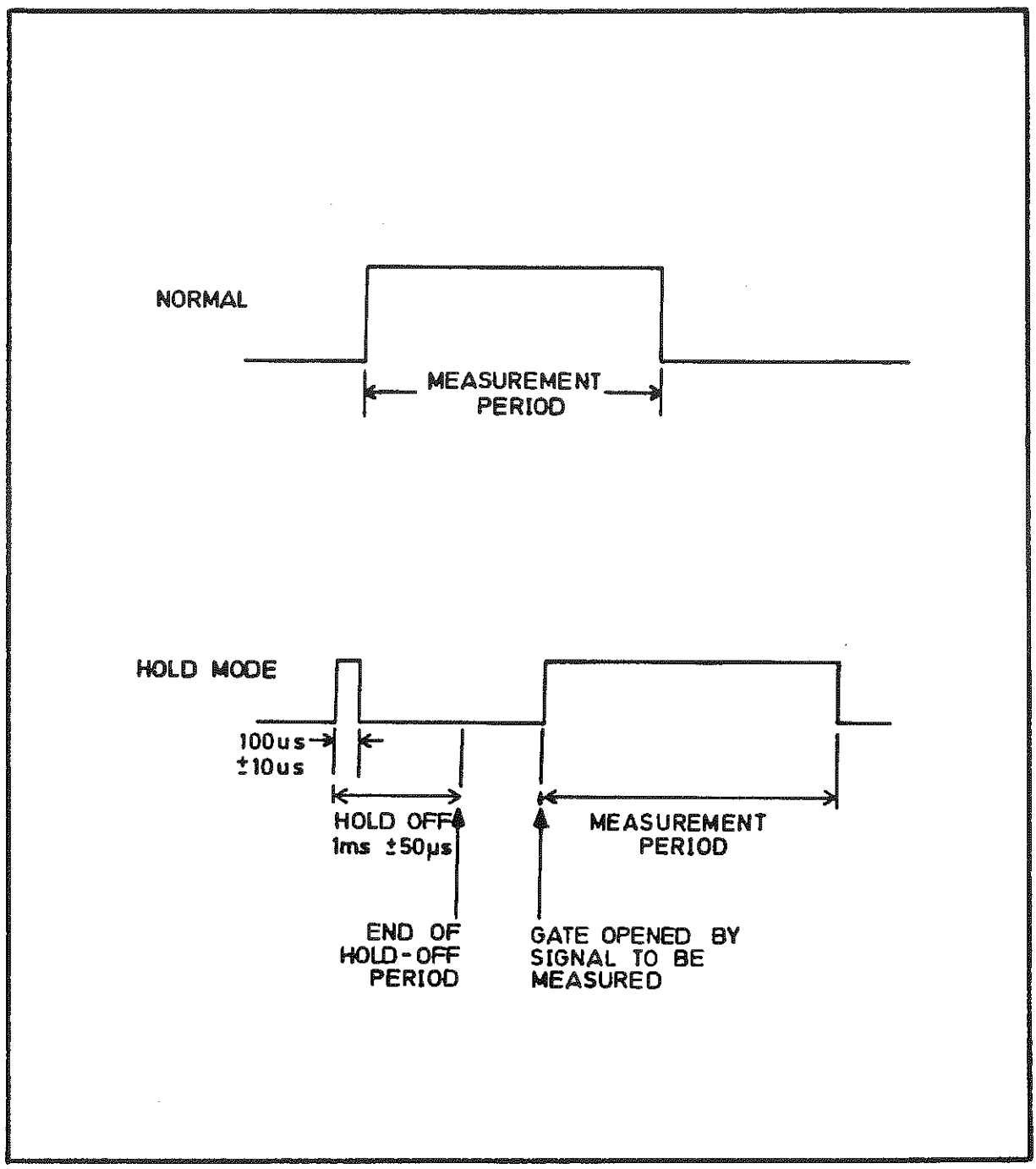


Fig. 4.1 Gate Output Waveforms

ERROR CODES

27 The instrument is able to detect a number of error states, which are indicated on the display. The meanings of the error codes are shown in Table 4.2.

TABLE 4.2

Error Codes

Display	Error
Er 02	Measurement result too large for the display.
Er 03	Overflow of internal counters.
Er 05	Programming error (GPIB only).
Er 50	Incorrect result obtained when in check mode.
Er 61	RAM failure.

Clearing the Error Codes

28 Error codes Er 02 and Er 03 are cleared by:

(1) Obtaining a measurement result that is within range.

(2) Selecting another measurement function.

USING THE BATTERY PACK OPTION

WARNING: LETHAL VOLTAGE
IF MEASUREMENTS ARE MADE ON SIGNAL SOURCES AT VOLTAGES ABOVE 50 V DC WITH THE INSTRUMENT POWERED FROM THE INTERNAL BATTERY OR AN EXTERNAL DC SUPPLY THE GROUND CONNECTOR OF THE AC POWER INPUT MUST BE CONNECTED TO GROUND.

Power Supply Changeover

29 When the battery pack option is installed, the instrument can be powered from the internal battery, an external DC supply of 11 V to 16 V, or an external AC supply. If the instrument is operating from either the external DC supply or the battery, it will automatically change to operation from the AC supply when this is connected. To prevent accidental battery discharge, the battery will not take over from either the AC or DC supply if that supply fails. An external DC supply will not take over from the AC supply if the AC supply fails.

Battery-Low Indication

30 When the instrument is operating from the internal battery, or from an external DC supply, the STBY/CHRG indicator will start to flash as the supply voltage approaches the minimum permissible level. This occurs regardless of whether the instrument is in the standby mode or not. When operating from the battery, the instrument can be used in the measurement mode for approximately 15 minutes after the indicator commences flashing.

31 When the voltage of the battery or the external DC supply reaches the minimum permissible level, the instrument shuts down completely.

Operating Instructions

32 Instructions for preparing the instrument to make measurements are given in the following paragraphs. No other change in the operating procedure is required.

Operating From the Battery

33 (1) Set the internal/external switch on the rear panel to INTERNAL BATTERIES.

(2) Set the BATTERY SAVE/NORMAL switch to NORMAL.

(3) Switch the instrument on.

(4) Check that the instrument goes through the normal switch-on sequence. If the STBY indicator is flashing, or if there is no display, charge the battery.

34 If the battery-save facility is to be used, set the BATTERY SAVE/NORMAL switch to BATTERY SAVE. The instrument will remain in the measurement mode for approximately one minute and will then switch to standby. It can be returned to the measurement mode for a further period of one minute by pressing the STBY/CHRG key.

Operation From an External DC Supply

35 (1) Ensure that the instrument is switched off.

(2) Connect the DC supply to the DC power-input plug on the rear panel. The mating connector is a 2.1 mm coaxial socket.

CAUTION: SUPPLY POLARITY
THE POSITIVE SIDE OF THE SUPPLY MUST BE CONNECTED TO THE CENTRE CONDUCTOR.

(3) Set the internal/external switch on the rear panel to EXTERNAL 11-16 V DC.

(4) Switch the instrument on. Check that the instrument goes through the normal switch-on sequence.

If the external DC supply is interrupted the instrument will not necessarily power-up again when the supply voltage is restored. In this event, switch off and then on again using the front-panel POWER switch.

Battery Charging

36 The battery is trickle-charged whenever the instrument is operated from an AC supply and the internal/external switch is at INTERNAL BATTERIES. To charge the battery at the full rate, connect the instrument to an external AC or DC supply, switch on and select the standby mode.

SECTION 5 OPERATION VIA THE GPIB

INTRODUCTION

1 The instrument must be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the AC line voltage selector.

GPIB OPERATING MODES

2 The instrument can be operated via the GPIB in either the addressed mode or the talk-only mode.

TALK-ONLY MODE

3 The talk-only mode may be used in systems which do not include a controller. Such a system permits remote reading of the instrument's measurement data, but the instrument is operated by means of the front-panel controls as described in Section 4.

4 The rate at which measurements are made is determined by the instrument. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if this has not been transferred to the listener.

5 The transfer of data from the instrument to the listener is triggered by the listener. The instrument's output buffer is cleared when the data transfer is complete. Problems arising from the differences between the measurement rate and data transfer trigger rate are resolved according to the following protocol:

(1) If data transfer is in progress at the end of a measurement cycle, the updating of the output buffer is delayed. The data transferred will relate to the previous measurement cycle.

(2) If the data transfer trigger occurs during a measurement cycle and the output buffer is empty, data transfer will be delayed until the buffer is updated. The data transferred will then relate to the latest measurement cycle.

(3) If a measurement cycle is completed before the results of the previous cycle have been transferred to the listener, the buffer will be updated. The data for the previous cycle will be overwritten and lost.

6 The rate at which measurements are made can be controlled in the following ways:

(1) The gate time of the instrument (duration of the measurement cycle) can be controlled by choosing an appropriate display resolution.

(2) The instrument can be operated in the hold mode. Single measurement cycles can be triggered, when required, by means of the RESET key.

7 The format of the data output is described in Table 5.1

ADDRESSED MODE

8 In addressed-mode operation, all the instrument's functions, except the channel A sensitivity potentiometer setting and the power ON/OFF and standby switching, can be controlled by means of device-dependent commands, sent via the bus, when the instrument is addressed to listen. The measurements made, and data regarding the instrument's status, can be read via the bus when the instrument is addressed to talk. If the instrument is addressed to talk when the output buffer is empty, no data transfer can take place and bus activity will cease. Data transfer will commence when the output buffer is updated at the end of the next measurement cycle.

DATA OUTPUT FORMAT

9 The same output message format is used for the transmission of measured values and numbers recalled from the instrument's internal stores. The message consists of a string of 21 ASCII characters for each value transmitted. These are to be interpreted as shown in Table 5.1. The units should be assumed to be Hz, seconds, or a ratio, depending upon the commands previously given to the instrument.

DEFERRED COMMANDS AND IMMEDIATE COMMANDS

10 Some commands (known as Deferred Commands) are accepted until a terminating character or message is received, see Table 5.5. The whole string will then be obeyed. Other commands (known as Immediate Commands) are obeyed as soon as they are received. These are indicated, in Table 5.16, by an asterisk.

Example: OUTPUT 716; FA ALI SRS85 S81 CR LF

Because SRS is an immediate command, Frequency A, A Channel Negative Slope, and 5 digit Resolution will be set following receipt of SRS5.

TABLE 5.1

Output Message Format

Byte No	Interpretation	Permitted ASCII Characters
1	Function letter	See Table 5.2
2	Function letter	
3	Sign of measurement	+ or -
4	Most significant digit	0 to 9
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Digit	0 to 9 or .
12	Digit	0 to 9 or .
13	Digit	0 to 9 or .
14	Digit	0 to 9 or .
15	Least significant digit	0 to 9 or .
16	Exponent indicator	E
17	Sign of exponent	+ or -
18	More significant digit	0 to 9
19	Less significant digit	0 to 9
20	Carriage return	CR
21	Line Feed	LF

NOTE 1:
Bytes 4 to 15 will always include 11 digits and a decimal point. Zeros will be added, where necessary, in the more significant digit positions.

NOTE 2:
The exponent indicated by bytes 18 and 19 will always be a multiple of three.

NOTE 3: (1999 only)
When B input is overloaded the frequency result will read 9.999999999 GHz.

TABLE 5.2

Function Letters

Function	Function Letters
Frequency A	FA
Frequency B	FB
Ratio A/D	RA
Ratio B/A (1998 only)	RB
Period A	PA
Check	CK
Recalled Data	**Function Letters**
Unit type	UT
Resolution	RS
Null store	NS
Special function	SF
Master software issue number	MS
GPIB software issue number	GS

NOTE:
Spaces are substituted for the function letters when special function S81 is active.

SERVICE REQUEST

11 The instrument can be set, by means of device-dependent commands, to generate the service request message (SRQ) when:

(1) A measurement cycle is completed.
(2) A change of frequency standard occurs.
(3) An error state is detected.
(4) Any combination of (1), (2) and (3).

12 The generation of the SRQ may also be inhibited. The necessary commands are given in Table 5.15. Option (3) of Paragraph 11 is selected when the instrument is first switched on.

STATUS BYTE

The format of the status byte, generated in response to a serial poll, is given in Table 5.3.

TABLE 5.3

Status Byte Format

DIO Line	Function
1 2 3	LSB ┐ ├ Number of error detected (binary) MSB ┘ (See NOTE 1)
4	'1' = frequency standard changed
5	'1' = reading ready (See NOTE 2)
6	'1' = error detected
7	'1' = service requested
8	'1' = gate open

NOTE 1:
The error code numbers which can occur are:

2 Result out of range of the display.
3 Overflow of internal counters.
4 Error in numerical entry.
5 Syntax error in GPIB command.

No measurement data string is available if error code 2 or 3 is generated.

NOTE 2:
Regardless of the SRQ mode in use, the SRQ message that a reading is ready is not generated following a data-recall operation.

NOTE 3:
The errors are cleared as follows:

Error 2: The error is cleared when an in-range measurement is completed.

Error 3: The error is cleared when an in-range measurement is completed.

Error 4: The error is cleared when a valid numerical entry is made.

Error 5: The command string will be correctly executed up to the point at which the error occurs. The remainder of the string will be hand-shaken, but not executed. The error is cleared when the next valid command is received.

EXPLANATION OF RESPONSE TO INTERFACE MESSAGES

14 The instrument will respond to all valid device-dependent commands which are received after it has been addressed to listen. Device-dependent commands are recognised as such because they are transmitted with the attention (ATN) message false.

15 The instrument also responds to a number of multi-line interface messages. These are recognised because they are transmitted with the ATN message true. Table 5.4 gives the instrument's response to different bus messages. The following paragraphs detail the instrument's response to these messages. Any multi-line message not specifically mentioned is hand-shaken, but is otherwise ignored.

Address Messages

16 The instrument responds to address messages defined by the setting of the address switches, A1 to A5, on the rear panel.

17 On receipt of its listen address, the instrument becomes a listener. If it has previously been addressed to talk it ceases to act as a talker. If in the local control state when the address is received, the instrument goes to the remote control state provided that the REN message is true.

18 On receipt of its talk address, the instrument becomes a talker. If it has previously been addressed to listen it ceases to act as a listener. If in the local control state when the address is received, it will remain under local control.

19 If the instrument has been addressed to talk, and then receives the talk address of another device, it ceases to act as a talker.

Local Lockout

20 The instrument will respond to the local lockout (LLO) message regardless of its addressed state. The return-to-local function of the LOCAL key on the front panel is disabled (the RESET/CONTINUE function remains enabled when in local control).

21 Local lockout is cleared by sending the remote enable (REN) message false. This returns all devices on the bus to the local control state.

Device Clear and Selected Device Clear

22 The instrument only responds to the device clear (DCL) message and the selected device clear (SDC) message when it is in the remote control state. It will only respond to the SDC message if it is a listener, but will respond to the DCL message regardless of its addressed state.

23 The instrument responds to either message by reverting to the functions and settings of the power-up state. No change is made to the condition of the GPIB interface.

TABLE 5.4

Response to Bus Messages

Message	Addressed State	Instrument Response
Address	Any	For listen address: Becomes a listener and goes to the remote control state. If previously addressed to talk, ceases to act as a talker. For talk address: Becomes a talker. If previously addressed to listen, ceases to be a listener. For talk address of another device: If previously addressed to talk, ceases to be a talker.
Local Lockout (LLO)	Any	LOCAL key disabled. (Cleared by sending the REN message false).
Device Clear (DCL) Selected Device Clear (SDC)	Any, but must be in remote control. Listen and in remote control	Reverts to power-up state.
Serial Poll Enable (SPE)	Any	Enters the serial poll mode state (SPMS). If addressed to talk while in this state, sends the status byte.
Serial Poll Disable (SPD)	Any	Enters the serial poll idle state (SPIS). If addressed to talk while in this state, sends data in the output message format.
Group Execute Trigger (GET)	Listen, and no measurement cycle in progress	Takes a measurement.
Go to Local (GTL)	Listen	Reverts to local control.
Untalk Unlisten	Talk Listen	Ceases to be a talker. Ceases to be a listener. The ADDR indicator is turned off.

Serial Poll Enable and Serial Poll Disable

24 The instrument responds to both the serial poll enable (SPE) message and the serial poll disable (SPD) message regardless of its addressed state.

25 The instrument responds to the SPE message by entering the serial poll mode state (SPMS). If the instrument is addressed to talk while in this state, it will put its status byte onto the bus instead of its normal data output string.

26 The instrument responds to the SPD message by leaving the SPMS and entering the serial poll idle state (SPIS). If the instrument is addressed to talk while in this state, it will put its data output string onto the bus provided data is available in the output buffer.

Group Execute Trigger

27 The instrument responds to the group execute trigger (GET) message provided that it is a listener and no measurement cycle is in progress. Except for the inability to retrigger during a measurement cycle, the response to the GET message is the same as to the device-dependent command T2.

Go to Local

28 The instrument responds to the go to local (GTL) message provided that it is a listener. The instrument reverts to the local control state, but remains addressed to listen. It will return to remote control on receipt of the first byte of a device-dependent command.

Untalk and Unlisten

29 If addressed to talk, the instrument will go to the talker idle state (TIDS) on receipt of the untalk message. If addressed to listen, it will go to the listener idle status (LIDS) on receipt of the unlisten message. The ADDR indicator will be turned off.

INPUT COMMAND CODES

29 When the instrument is addressed to listen it can be controlled by means of device-dependent commands given in Table 5.6 to 5.15. All the device-dependent commands are listed in alphabetic order in Table 5.16.

31 If more than one command is to be sent, no delimiters are required. If necessary, commas, spaces and semicolons may be included in command strings as an aid to clarity without affecting the operating of the instrument. Each command string must be followed by an end-of-string terminating group. The permitted terminating groups are shown in Table 5.5.

TABLE 5.5

Permitted Terminators

1	2	3	4	5	6
LF	LF EOI true	CR EOI true	CR LF	CR LF EOI true	Last Character EOI true

NOTE: LF = Line feed
CR = Carriage return

TABLE 5.6

Instrument Preset Code

Function	Code
Set instrument functions and settings to the power-up state	IP

TABLE 5.7

Measurement Function Codes

Function	Code
Frequency A	FA
Frequency B	FB
Period A	PA
Ratio A/D	RA
Ratio B/A (1998 only)	RB
Check	CK

TABLE 5.8

Input Control Codes (Channel A)

Function	Code
1 MΩ input impedance selected	AHI
50 Ω input impedance selected	ALI
Positive pulse offset (M/S ratio less than 1:2.5) selected	APS
Sinewave offset (M/S ratio between 1:2.5 and 2.5:1) selected	ASS
Negative pulse offset (M/S ratio more than 2.5:1) selected	ANS
X20 attenuator disabled	AAD
X20 attenuator eanabled	AAE
Channel A filtering enabled	AFE
Channel A filtering disabled	AFD

TABLE 5.9

Measurement Control Codes

Function	Code
Select continuous measurement mode	TØ (see NOTE 1)
Select one-shot measurement mode	T1 (see NOTE 2)
Take one measurement	T2
Null disabled	ND
Null enabled	NE
Reset (Stop measurement cycle and clear output buffer)	RE

NOTE 1:
When making continuous measurements the output buffer is updated at the end of each gate period. If the buffer is being read via the GPIB when the gate period ends, updating is delayed until reading is complete.

NOTE 2:
When one-shot measurements are being made, the output buffer is cleared each time command T2 is received. The measurement made must, therefore, be read before a further measurement cycle is triggered.

TABLE 5.10

Store and Recall Codes

Function	Code
Recall unit type	RUT
Store display resolution number	SRS
Recall display resolution number	RRS
Store null value	SN
Recall null value	RN
Recall special function register	RSF
Recall master software issue number	RMS
Recall GPIB software issue number	RGS

NOTE 1:
Numbers to be stored should follow the store command. The format to be used for numerical entry is given in Table 5.11. The limiting values for numerical entries are given in Table 5.12.

NOTE 2:
The instrument returns to the measurement mode automatically at the completion of a store or recall operation.

NOTE 3:
No SRQ message is generated for recalled data.

TABLE 5.11

Numerical Input Format

Byte No	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	+ or -
2	Most significant digit	0 to 9 or .
3	Digit	0 to 9 or .
4	Digit	0 to 9 or .
5	Digit	0 to 9 or .
6	Digit	0 to 9 or .
7	Digit	0 to 9 or .
8	Digit	0 to 9 or .
9	Digit	0 to 9 or .
10	Digit	0 to 9 or .
11	Digit	0 to 9 or .
12	Least significant digit	0 to 9 or .
13	Exponent indicator	E or e
14	Sign of exponent	Space, + or -
15	More significant digit	0 to 9
16	Less significant digit	0 to 9

NOTE 1:
Spaces, nulls or zeros occurring immediately before byte 1 will be ignored.

NOTE 2:
Byte 1 may be omitted. A positive mantissa will then be assumed.

NOTE 3:
Bytes 2 to 12 may contain up to ten digits and a decimal point. If more than ten digits are entered without a decimal point, excess digits will be truncated. The excess digits will, however, increase the power of ten stored.

If fewer than ten digits are required the unused bytes may be omitted.

NOTE 4:
Spaces or nulls entered between bytes 12 and 13 will be ignored.

NOTE 5:
The exponent group, bytes 13 to 16, may be omitted.

NOTE 6:
Byte 14 may be omitted or transmitted as a space. In either case a positive exponent will be assumed.

NOTE 7:
Byte 16 may be omitted for a single-digit exponent.

TABLE 5.12

Numerical Input Range

Function	Command Code	Numerical Limits	
		Low	High
Null Store	SN	1×10^{-9}	1×10^{10}
		0	
		-1×10^{10}	-1×10^{-9}

TABLE 5.13

Gate Times

Number of digits in Freq. Period and Check	Gate Time	Resolution Number
10	20 s	10
9	1 s	9
8	100 ms	8
7	10 ms	7
6	1 ms	6
5	1 ms	5
4	1 ms	4
3	1 ms	3

TABLE 5.14

Special Function Codes

Function	Code
Internal arm	S10
External arm	S11
Basic 10 MHz check	S70
Indicators check	S71
These codes are reserved for diagnostic purposes and are described in the Maintenance Manual	S72 S73 S74 S75
Leading (function) letters in O/P string	S80
No leading (function) letters in output string	S81

NOTE:
Special functions 71 to 75 can be entered into the special functions register at any time. They are active only when the instrument is in the Check mode.

TABLE 5.15

Service Request Codes

Function	Code
Inhibit generation of SRQ	QØ
SRQ generated when error is detected	Q1
SRQ generated for measurement ready	Q2
SRQ generated for measurement ready or error detected	Q3
SRQ generated for frequency standard changeover	Q4
SRQ generated for frequency standard changeover or error detected	Q5
SRQ generated for measurement or frequency standard changeover	Q6
SRQ generated for measurement ready, error detected or frequency standard changeover	Q7

NOTE:
SRQ is not generated by data recalled from store.

TABLE 5.16

Alphabetic List of Command Codes

	Code		Code		
	AAD	A channel X20 attenuator disabled	PA	Period A	
	AAE	A channel X20 attenuator enabled	Qn	SRQ mode	*
	AFD	A channel filtering disabled	RA	Ratio A/D	
	AFE	A channel filtering enabled	RB	Ratio B/A (1998 only)	
	AHI	A channel, 1 MΩ	RE	Reset measurement	
	ALI	A channel, 50 Ω	RGS	Recall GPIB software issue	*
	ANS	A channel, negative pulse offset	RMS	Recall master software issue number	*
	APS	A channel, positive pulse offset	RN	Recall null value	*
	ASS	A channel sinewave offset	RRS	Recall resolution	*
	CK	Check	RSF	Recall special function	*
	FA	Frequency A	RUT	Recall unit type	*
	FB	Frequency B	Snn	Special function	
*	IP	Instrument preset	SN	Store null value	*
*	ND	Null disabled	SRS	Store resolution	*
*	NE	Null enabled	Tn	Measurement mode or trigger a reading	

NOTE:
n represents a single digit.
* indicates an Immediate mode command. (See Page 5-2).

SECTION 6 PRINCIPLES OF OPERATION

INTRODUCTION

1 This section describes the principles of operation of the instruments, with respect to a number of block diagrams in the text, and describes the significant features of the circuits used with respect to the circuit diagrams given in Section 8. The block diagrams are annotated with the main circuit references to simplify cross referencing between the block diagram and circuit diagram.

2 In the circuit descriptions the integrated circuits are referred to by the circuit reference given on the appropriate circuit diagram. Note that a separate series of numbers, starting at IC1, is allocated to each assembly. Where an integrated circuit package contains more than one circuit, suffix letters are used to distinguish between them. Where it is required to identify a particular pin of an integrated circuit, the circuit reference, with suffix letter if appropriate, is followed by an oblique stroke and the required pin number.

FUNCTIONAL SYSTEMS

3 The instruments contain a number of functional systems, unless otherwise stated these are common to both instruments. The systems are:

(1) The channel A system.

(2) The 1998 channel B system.

(3) The 1999 channel B system.

(4) The measurement system.

(5) The display system.

(6) The keyboard system.

(7) The microprocessor system.

(8) The standby and IRQ system.

(9) The power supply system.

(10) The internal frequency standard system.

4 The functional relationship between the systems is illustrated in Fig 6.1. The measurement system is internally configured by the microprocessor system according to the instructions entered via the keyboard or GPIB system. The signal to be measured and the signal from the frequency standard are fed to the measurement system. The measured result is passed to the microprocessor system. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed to the display or GPIB system.

5 The standby and IRQ system handles instructions to switch to standby, received from the keyboard system or the battery pack option, and interrupt requests made by other systems.

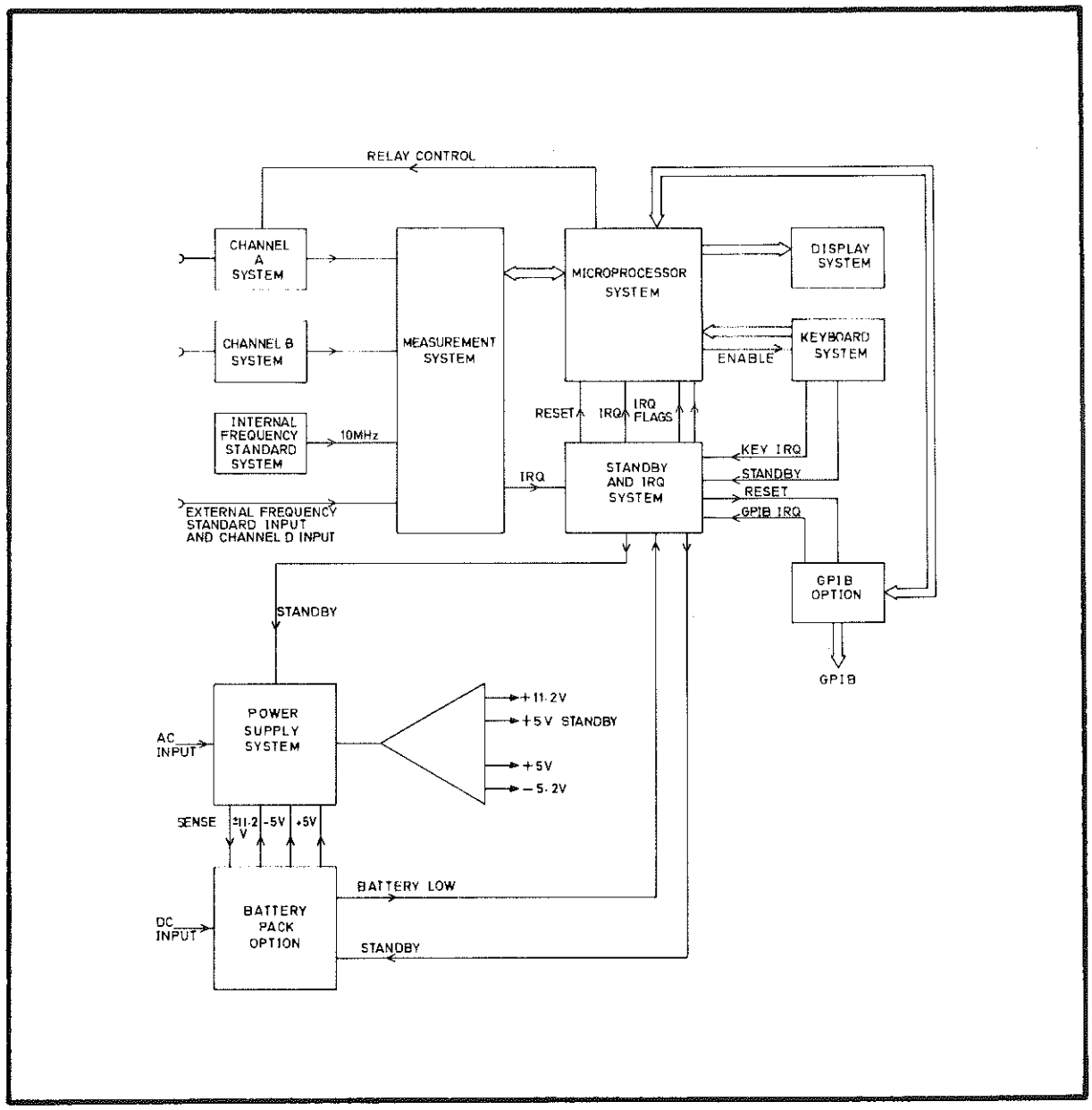


Fig 6.1 Functional Block Diagram

THE CHANNEL A SYSTEM

Functional Description

6 The channel A system processes the signals applied at the A channel input to produce a differential pair of signals which are fed to the measurement system. A block diagram is given in Fig 6.2.

7 The channel includes relay-controlled circuits which allow selection of 50 Ω/1 MΩ input impedance and X1/X20 attenuation. Signal filtering can be introduced to reduce the bandwidth of the amplifier to 50 kHz nominal.

8 A continuously variable SENSITIVITY control, adjustable from the front panel, is provided.

9 The differential output is taken from a Schmitt trigger comparator. The trigger level at the comparator input is normally 0 V, but can be offset to be positive or negative.

10 Control signals for the system relays and trigger level control are supplied from the microprocessor system.

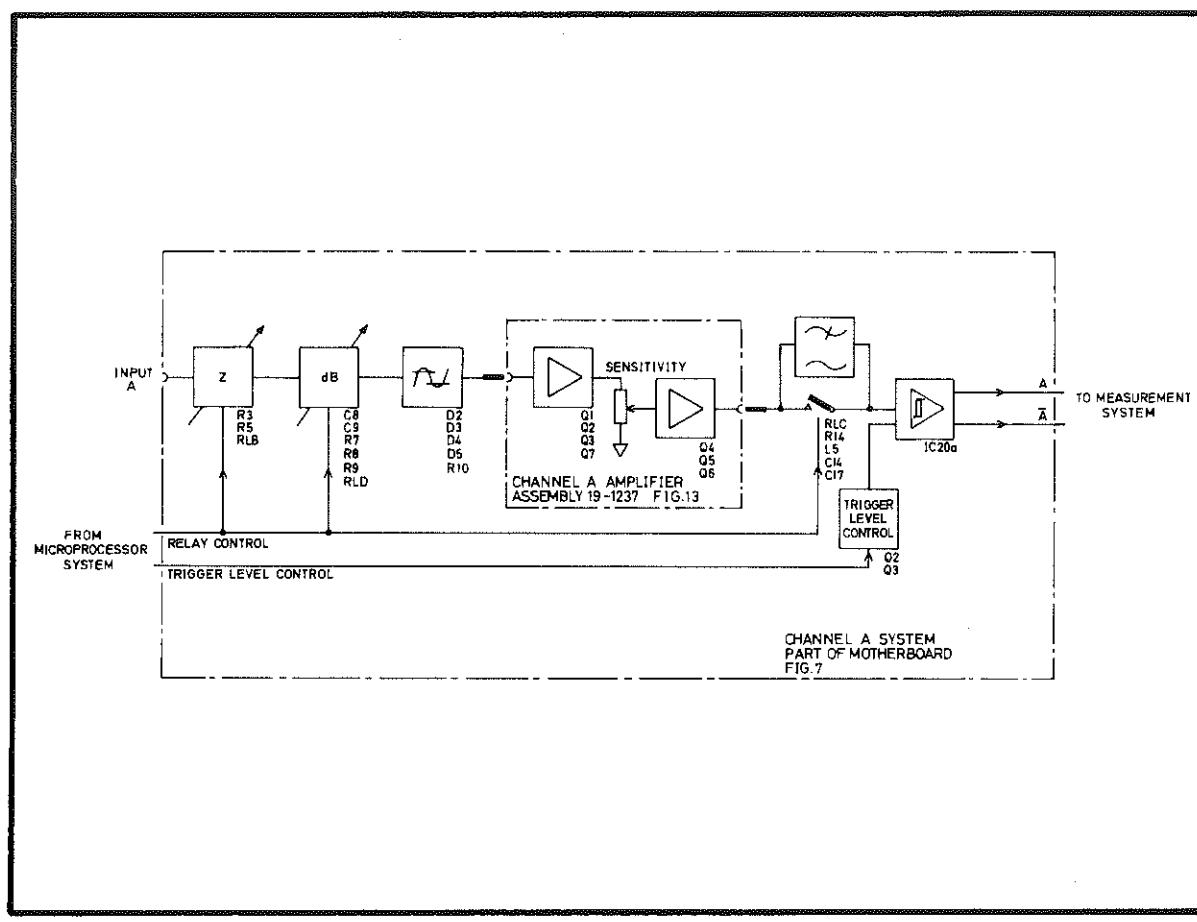


Fig 6.2 The Channel A System

Circuit Description

11 The circuit diagram is shown in Fig 7 and Fig 13 in Section 8. When relay RLB is energised the input impedance seen at SK5 (INPUT A) is 50 Ω, given by resistors R3/R5 in parallel.

12 The X1/X20 attenuator is formed by R7, R8, C8, C9 and RLD. With RLD de-energised, the attenuator has a series eleement R7 and a shunt element formed by R8 and R9 in parallel. The attenuation is 26 dB (nominal). With RLD energised R7 is short circuited, giving 0 dB attenuation.

13 The signal is limited to approximately ± 1.5 V by the diodes D2 to D5, and is passed to the A channel amplifier via PL23 pin 3. The limiter prevents damage to the amplifier input due to excessive voltage swing while maintaining the sharp edges of the signal.

14 The amplifier has a high input impedance, provided by the FET Q1, which is connected as a source follower. The output from Q1 drives the emitter follower Q3, which provides a low impedance drive for the SENSITIVITY control, R7 and R8. Constant current sinks for Q1 and Q3 are provided by Q2 and Q7.

15 The current in Q1 can be adjusted by means of R4. This allows the no-signal voltage at the emitter of Q3 to be set to 0 V, so that the following stage is correctly biased. The gain from SK23 pin 3 to the emitter of Q3 is approximately -2 dB at low frequencies, and falls with increasing frequency.

16 The signal from the SENSITIVITY control is amplified in the long-tailed-pair circuit, Q4/Q5, and is fed back to the motherboard via the emitter follower Q6 and SK23 pin 9.

17 The amplified signal is limited to approximately ± 800 mV. For output amplitudes below this level, the gain from the wiper of R7 to the emitter of Q6 is approximately 6 dB at low frequencies.

18 With RLC de-energised, the signal from SK23 pin 9 is connected directly to the comparator, IC20a. When the low-pass filter is enabled, RLC is energised and the filter, formed by R14/L5/C14/C17, is inserted in the signal path.

19 The comparator compares the signal at IC20a/7 with the trigger level voltage at IC20a/8. The hysteresis of the comparator is adjusted by means of R24 to be approxiamtely ± 7 mV relative to the trigger level.

20 The trigger level is controlled by Q2 and Q3. For sinewave inputs Q2 is switched on and Q3 switched off. The voltage at IC20a/8 is 0 V (set by means of R19). With positive pulse offset selected Q2 and Q3 are both on, and the resulting current in R23 gives a voltage of +15 mV at IC20a/8. When negative pulse offset is selected Q2 and Q3 are both off, and the resistor chain R23/R21/R19 gives a voltage of -15 mV at IC20a/8.

21 The differential outputs of IC20a are at ECL levels, and are fed to the measurement system.

22 The relays, Q2 and Q3 are controlled by the microprocessor system. The voltage levels on the control lines are latched in IC11, shown in Fig 8 in Section 8.

THE 1998 CHANNEL B SYSTEM

Functional Description

23 A block diagram of the system is given in Fig 6.3. The system processes the signal applied at the B channel input and feeds it to the measurement system.

24 The channel input is protected by a fuse, mounted in the input connector, and by a signal limiting circuit. This is followed by an automatic level control circuit, which reduces the range of signal level applied to the amplifier.

25 After amplification the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement system.

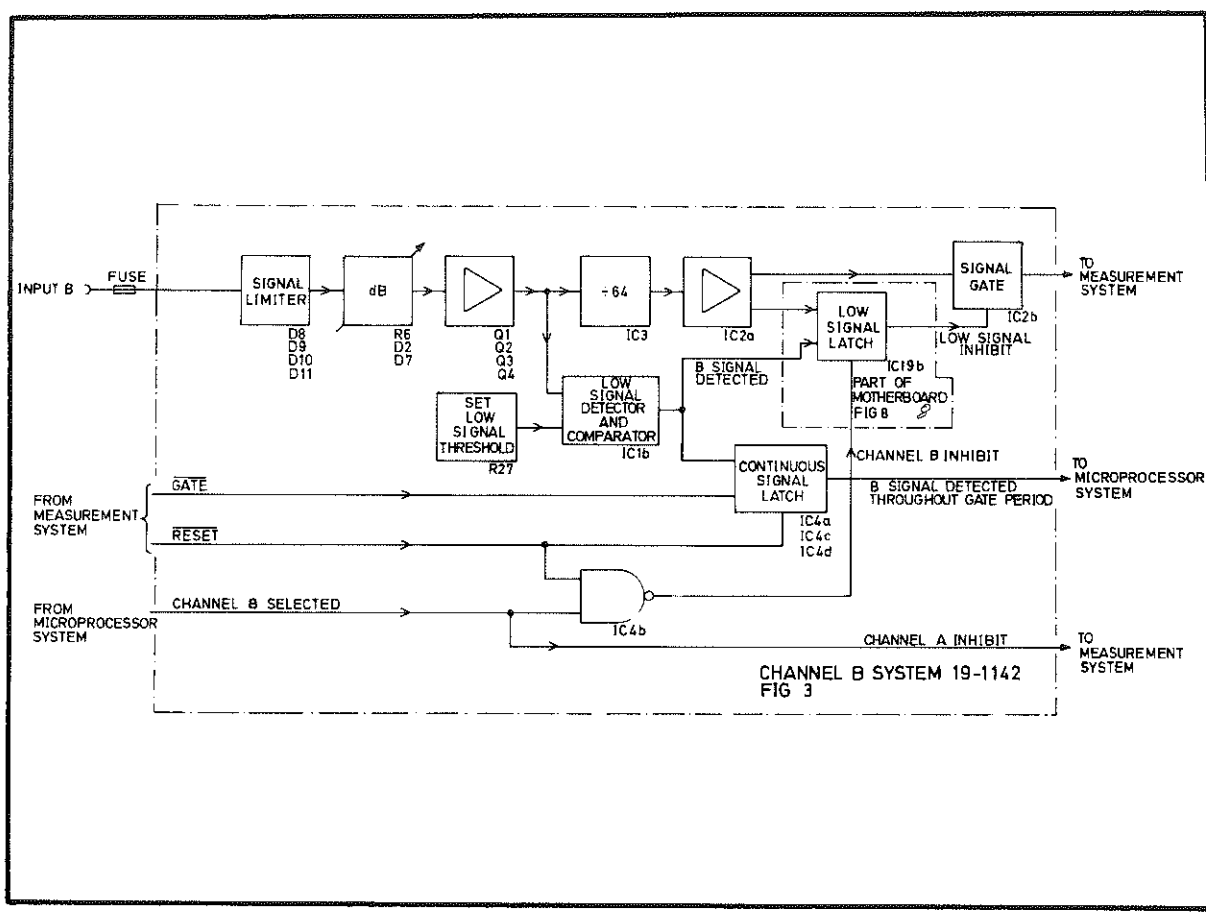


Fig 6.3 The 1998 Channel B System

26 The amplitude of the signal at the amplifier output is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold the low-signal latch is armed, and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on bursts of signal.

27 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period, and is set if the detector output falls below the threshold level. The microprocessor system samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

28 If B channel is not selected, the low-signal latch is held reset by a control signal from the microprocessor system and the output to the measurement system is inhibited.

Circuit Description

29 The circuit diagram is shown in Fig 3 in Section 8. The signal to be measured is connected at SK13 (INPUT B). The circuit is protected by the fuse, which is mounted within SK13. The signal amplitude is limited by the diode clamp comprising D8, D9, D10 and D11.

30 A measure of automatic gain control is achieved by means of an attenuator, formed by R6 and the impedance of the PIN diodes, D2 and D7. The peak-to-peak detector, D1, D3, R7 and C48, produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases, so that changes in signal amplitude are offset by changes in attenuation.

31 The signal passes through four amplifier stages, incorporating Q1, Q2, Q3 and Q4. The amplified signal is fed to the counter, IC3, via the shaping circuit formed by R37, C46 and R36.

32 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that B channel is selected and the amplitude of the signal is adequate, the output at IC2a/2 passes to the measurement system via the gate, IC2b, and SK7 pin 5.

33 The signal at the output of Q4 is fed to the low-signal detector, D5 and C23. The comparator, IC1b, compares the detector output with a threshold voltage, set by R27. The comparator output is at logic '1' if the detector output is below the threshold (channel B signal amplitude too low for accurate counting).

34 The logic level at the comparator output is inverted in IC1a, and is fed via SK7 pin 14 to the D input of the low-signal latch, IC19b, shown in Fig 10. IC19b is clocked by the output of IC2a via SK7 pin 8. If the signal from Q4 is below the threshold, IC19b/14 goes to logic '1'. This level is fed back via SK7 pin 7 to disable the gate, IC2b, and inhibit the output to the measurement system.

35 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC1c. The resulting signal and the output of the comparator, IC1b, are fed to IC4a. If both inputs are at logic '1', indicating that the channel B signal level is too low while the gate is open, the continuous signal latch, IC4c and d, is set. The latch output is fed to the microprocessor system via SK7 pin 11, and prevents the result of any measurement made during that gate period from being displayed.

36 The U signal at SK7 pin 16 is at logic '1' when channel B is selected. A buffered version of this signal is fed to SK7 pin 1 via IC2c, and disables channel A at IC19a, shown in Fig 10. When channel B is not selected, SK17 pin 16 is at logic '0'. This level is inverted and buffered in IC4b and IC1d, and is fed to IC19b, shown in Fig 10, via SK7 pin 13. IC19b is held reset, inhibiting the channel B signal at IC2b via SK7 pin 7.

THE 1999 CHANNEL B SYSTEM

Functional Description

37 A block diagram of the system is given in Fig 6.4. The system processes the signal applied at the B channel input and feeds it to the measurement system.

38 The input to amplifier IC2 is protected by a pin diode T attenuator. At very high signal levels the T attenuator is tripped into a high impedance state. At normal operating levels the attenuator is controlled to ensure that IC2 is not overdriven. After amplification the signal is prescaled by 256 before being passed via a buffer and a signal gate to the measurement system.

39 The amplitude of the signal output of IC5 is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold the low-signal latch is armed, and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on bursts of signal.

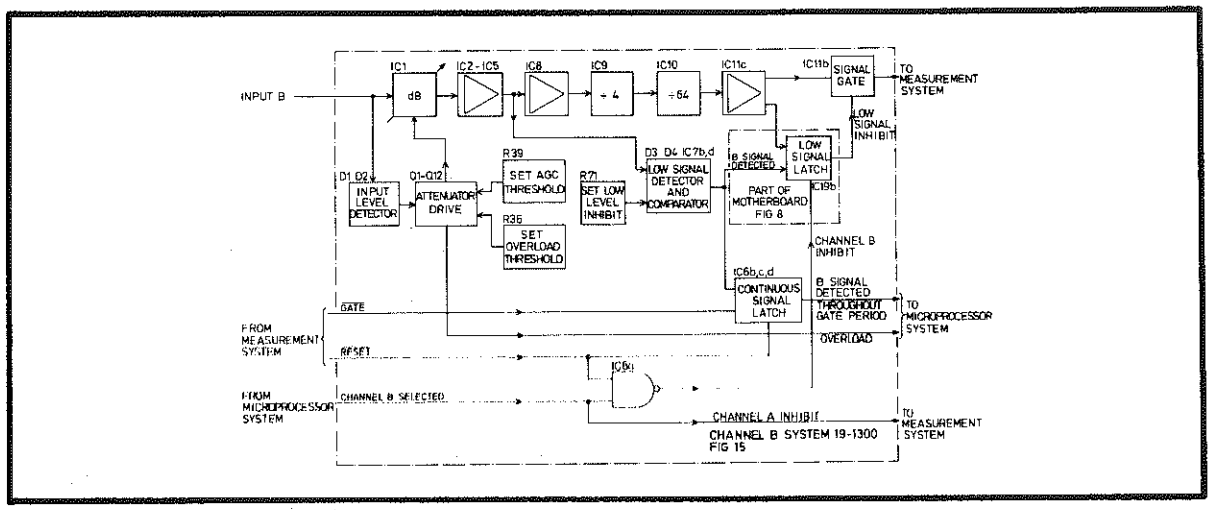


Fig 6.4 The 1999 Channel B System

40 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period, and is set if the detector output falls below the threshold level. The microprocessor system samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

41 If B channel is not selected, the low-signal latch is held reset by a control signal from the microprocessor system and the output to the measurement system is inhibited.

Circuit Description

42 The circuit diagram is shown in Fig 15 in Section 8. The signal to be measured is connected at the B INPUT on the front panel.

43 The input level is monitored by peak detector D1, C8, the voltage across C8 being amplified by Q1, Q2, Q4 and Q7. The amplified voltage controls the current drivers Q3, Q6 and Q9. Feeding an appropriate forward bias current through pin diode package IC1 scales the attenuation of the T network, of which IC1 is part, to prevent amplifier IC2 being overloaded. R39 sets the input level below which IC1 is at its minimum attenuation condition.

44 At input levels above maximum (see technical specification) set by R36, comparator Q5/Q8 changes state, turning off the series arm of the T attenuator via Q10. IC1 is then in a high attenuation condition. Q12 is turned on via Q11, taking SK7 pin 10 ($\overline{\text{O TRIP}}$) low, to signal overload to the microprocessor. With B channel selected, an overload condition results in the front panel OVERLOAD LED being lit and the numerical display indicating 9.999999999 GHz.

45 The signal passes through five amplifier stages consisting of IC1, IC2, IC3, IC4 and IC8. The amplified signal is fed to the counter IC9.

46 The signal frequency is prescaled by 4 in IC9, by 64 in IC10 and buffered in IC11c. Provided that B CHANNEL is selected, and the amplitude of the signal is adequate, the output of IC11c passes to the measurement system via IC11b and SK7 pin 5.

47 The signal at the output of IC5 is also fed to the low-signal detector D3 and C26. Comparator IC7d compares the detector output with a threshold voltage, set by R71. The comparator output is a logic 1 if the detector output is below the threshold, i.e. the B channel input signal amplitude is too low for accurate counting.

48 The logic level at the comparator output is inverted in IC7b, and is fed via SK7 pin 14 to the D input of the low-signal latch, IC19b, shown in Fig 10. IC19b is clocked by the output of IC11c via SK7 pin 8. If the signal from IC5 is below the threshold, IC19b/14 goes to logic '1'. This level is fed back via SK7 pin 7 to disable the gate, IC11c, and inhibit the output to the measurement system.

49 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC7c. The resulting signal and the output of the comparator, IC7d, are fed to IC6d. If both inputs are at logic '1', indicating that the channel B signal level is too low while the gate is open, the continuous signal latch, IC6b and 6c, is set. The latch output is fed to the microprocessor system via SK7 pin 11, and prevents the result of any measurement made during that gate period from being displayed.

50 The U signal at SK7 pin 16 is at logic '1' when channel B is selected. A buffered version of this signal is fed to SK7 pin 1 via IC11a, and disables channel A at IC19a, shown in Fig 10. When channel B is not selected, SK7 pin 16 is at logic '0'. This level is inverted and buffered in IC6a and IC7a and is fed to IC19b, shown in Fig 10, via SK7 pin 13. IC19b is held reset, inhibiting the channel B signal at IC11b via SK7 pin 7.

THE MEASUREMENT SYSTEM

Functional Description

51 The measurement circuits of the instrument are provided by three custom-built integrated circuits. These are the two Multiple Counter and Control (MCC) circuits, MCC1 and MCC2, and the Timing Error Correction (TEC) circuit. A block diagram is shown in Fig 6.5.

52 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function in use. The recipromatic counting technique is used. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown in Fig 6.6.

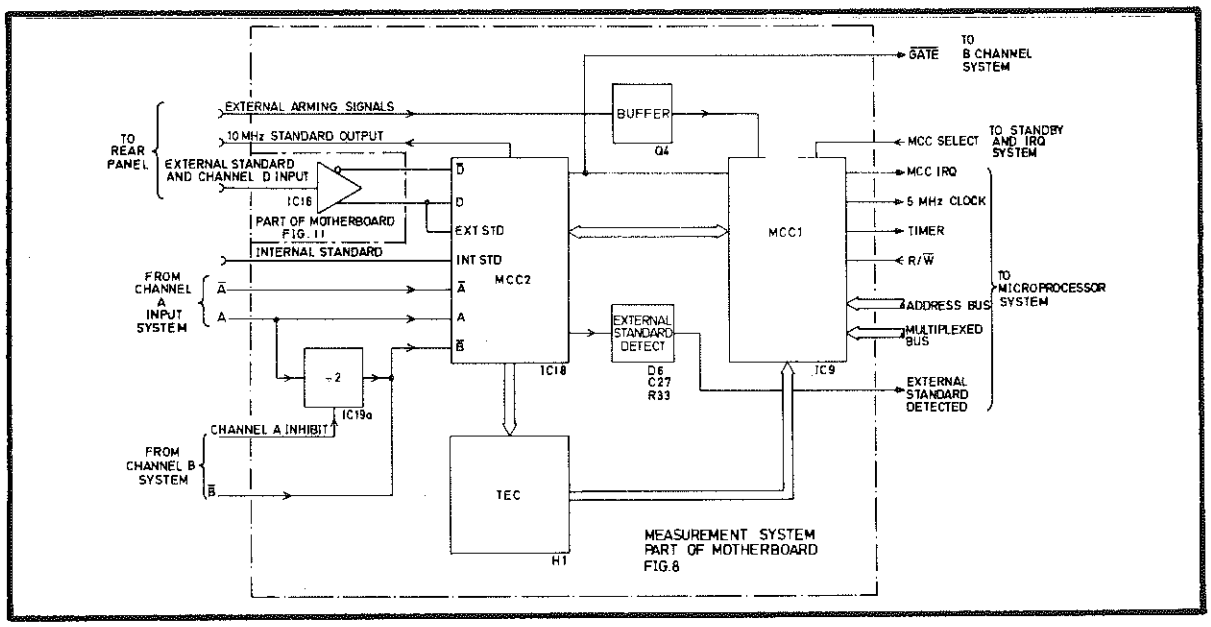


Fig 6.5 The Measurement System

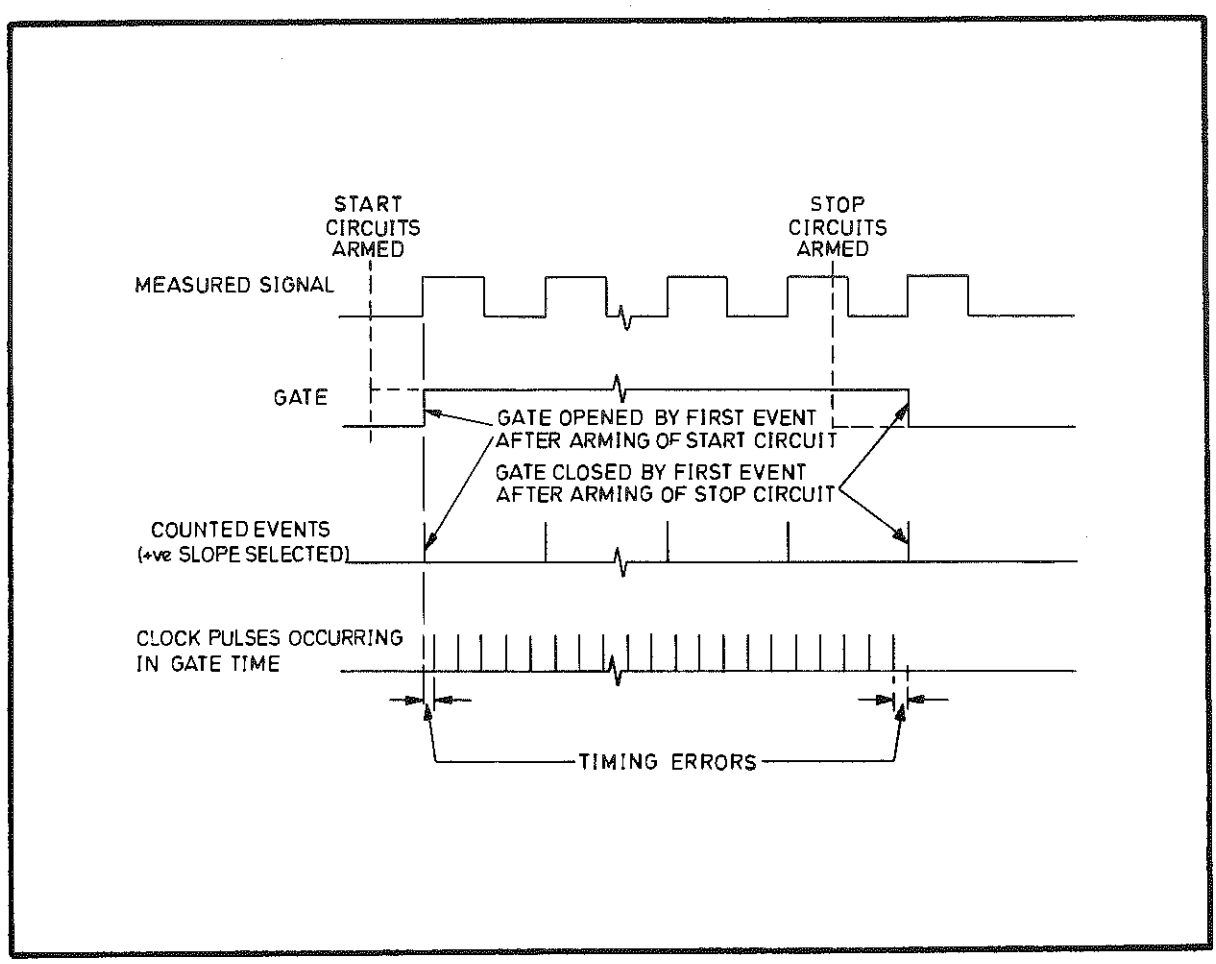


Fig 6.6 Basic Reciprocatic Counting Technique

The gate time therefore extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open. This leads to timing errors at both ends of the gate time, as shown. The TEC circuit enhances the measurement accuracy by compensating for these errors.

53 For FREQ A and PERIOD A with sinewave offset selected, the A channel signal is scaled by two and fed to the $\overline{B}$ input of MCC2. For all other measurement functions the channel A signal is fed to the A and $\overline{A}$ inputs of MCC2. When FREQ B is selected, the prescaler is disabled by the A CHANNEL INHIBIT signal from the B channel system.

54 At the end of each measurement period MCC1 generates an interrupt request for the microprocessor system. The registers within MCC1 are addressed using the address bus and the MCC SELECT line. The measured value is transferred to the microprocessor system via the multiplexed bus.

55 The internal and external frequency standard inputs are both fed to MCC2. The system will operate from the external standard provided that the input is of sufficient amplitude. A 10 MHz output, derived from the frequency standard in use, is made available at a socket on the rear panel.

Circuit Description

56 The circuit diagram is shown in Fig 8 in Section 8.

Measured Signal Input

57 For the FREQ A and PERIOD A measurement functions with sinewave offset selected, the channel A signal frequency is divided by 2 in IC19a and fed to IC18/19. For RATIO B/A, and when the offset is set for pulse, the differential A channel signals are fed to IC18/17 and 18.

58 For the FREQ B and RATIO B/A functions the $\overline{B}$ signal is fed to IC18/19. For these functions IC19a/5 is held at logic '1' by the PST1 control line (A CHANNEL INHIBIT) from the B channel system. As a result, IC19a is held set and the A signal is inhibited from reaching IC18/19. When the D channel is in use the differential signals are fed to IC18/15 and 16.

Reference Frequency

59 The internal reference signal is applied to IC18/2 and the external reference signal, if present, to IC18/3. A buffered version of the external reference is present at IC28/24, and is applied to the detector D6/C27/R33. The detector output is fed to IC13/6, and is read periodically by the microprocessor. If the level is above the TTL logic '1' threshold, the microprocessor sets IC18/38 to logic '0' and the measurement system switches to use the external reference.

60 A 10 MHz signal, derived from the frequency standard in use, is present at IC18/37, and is fed to the 10 MHz STD OUTPUT socket on the rear panel via PL19 pin 2.

61 A 10 MHz reference signal, derived from the frequency standard in use is present at IC18/36. This signal is applied to the TEC, H1, at pin 6, and, after inversion in IC10e, to IC9/24.

Microprocessor Clock and Timer

62 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if fitted) is taken from IC9/2. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC9/4.

Channel B Gate and Reset

63 A $\overline{\text{GATE}}$ signal (logic '0' during the measurement period) and a $\overline{\text{RESET}}$ signal (negative going pulse at the end of each measurement period) are taken from IC18/27 and IC9/40 and fed to the B channel system via PL7 pins 17 and 15.

External Arming Input

64 Signals connected to the EXT ARM INPUT socket on the rear panel are fed to IC9/27 via PL19 pin 1 and the amplifier stage, Q4.

Control Signals

65 The logic levels on lines Q0 and Q4, between IC18 and IC9 are shown in Table 6.1. These levels are stable if no signals are applied to any of the channel inputs.

TABLE 6.1

Control Signals

Measurement Function	Control Line				
	Q0	Q1	Q2	Q3	Q4
FREQ A	1	1	0	1	0
PERIOD A	1	1	0	1	0
FREQ B	1	1	0	1	0
RATIO A/D	1	1	0	1	1
RATIO B/A (1998 only)	1	0	1	1	1
CHECK EXT ARM (Special function 72)	1	1	1	0	1
CHECK RECALL (Special function 73)	1	1	1	0	0
CHECK NULL (Special function 74)	1	1	1	0	1
CHECK 50Ω/1MΩ (Special function 75)	1	1	1	0	0

THE DISPLAY SYSTEM

Functional Description

66 A block diagram of the system is given in Fig 6.7. The GPIB indicators, the GATE indicator and the STANDBY indicator are held on or off by control signals from other systems. The remainder of the display is multiplexed under the control of the display drivers.

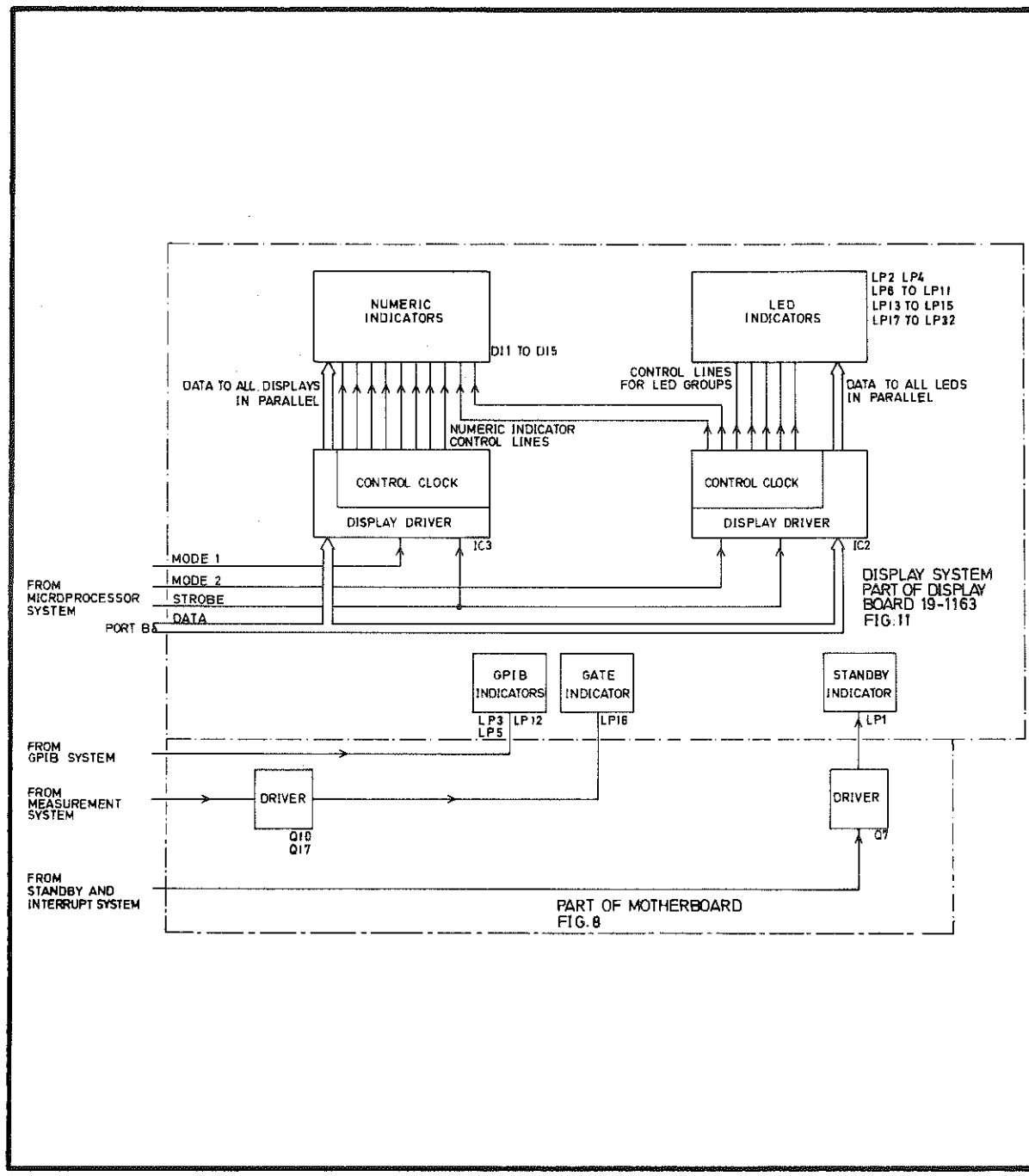


Fig 6.7 The Display System

67 To update the display, the microprocessor selects the appropriate display driver, using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into a memory within the display driver under the control of the STROBE signal.

68 The display driver puts the data words onto its output bus in turn. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

Circuit Description

69 The circuit diagram is shown in Fig 11 in Section 8. The GPIB indicators, LP3, LP5 and LP12, are driven via SK1 from the GPIB system. The GATE indicator, LP16, is driven from the measurement system via a driver stage, shown in Fig 10, and SK2 pin 11. The STANDBY indicator, LP1, is driven via SK1 pin 8 from the standby and interrupt system. The remaining LED indicators and the numeric indicator DI5 are controlled by the display driver, IC2. Numeric indicators DI1 to DI4 are controlled by IC3.

70 Display data are stored in memory within IC2 and IC3. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display drivers by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

71 The microprocessor then selects the display driver required by setting a logic '0' on the appropriate MODE line, at SK1 pin 3 or 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

72 The output of each display driver is multiplexed, under the control of an internal clock. Eight-bit display data (for seven segments + decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enablement line of the device or group of indicators which is to display the data. The enablement line waveforms consist of 500 µs positive-going pulses at approximately 250 pps.

THE KEYBOARD SYSTEM

Functional Description

73 A block diagram of the system is given in Fig 6.8. When a key is pressed the keyboard encoder generates a 4-bit word, corresponding to the position of the key within the matrix, without microprocessor action. An interrupt request (IRQ) is made to the microprocessor on the KEYBOARD DATA READY line when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE signal from the microprocessor.

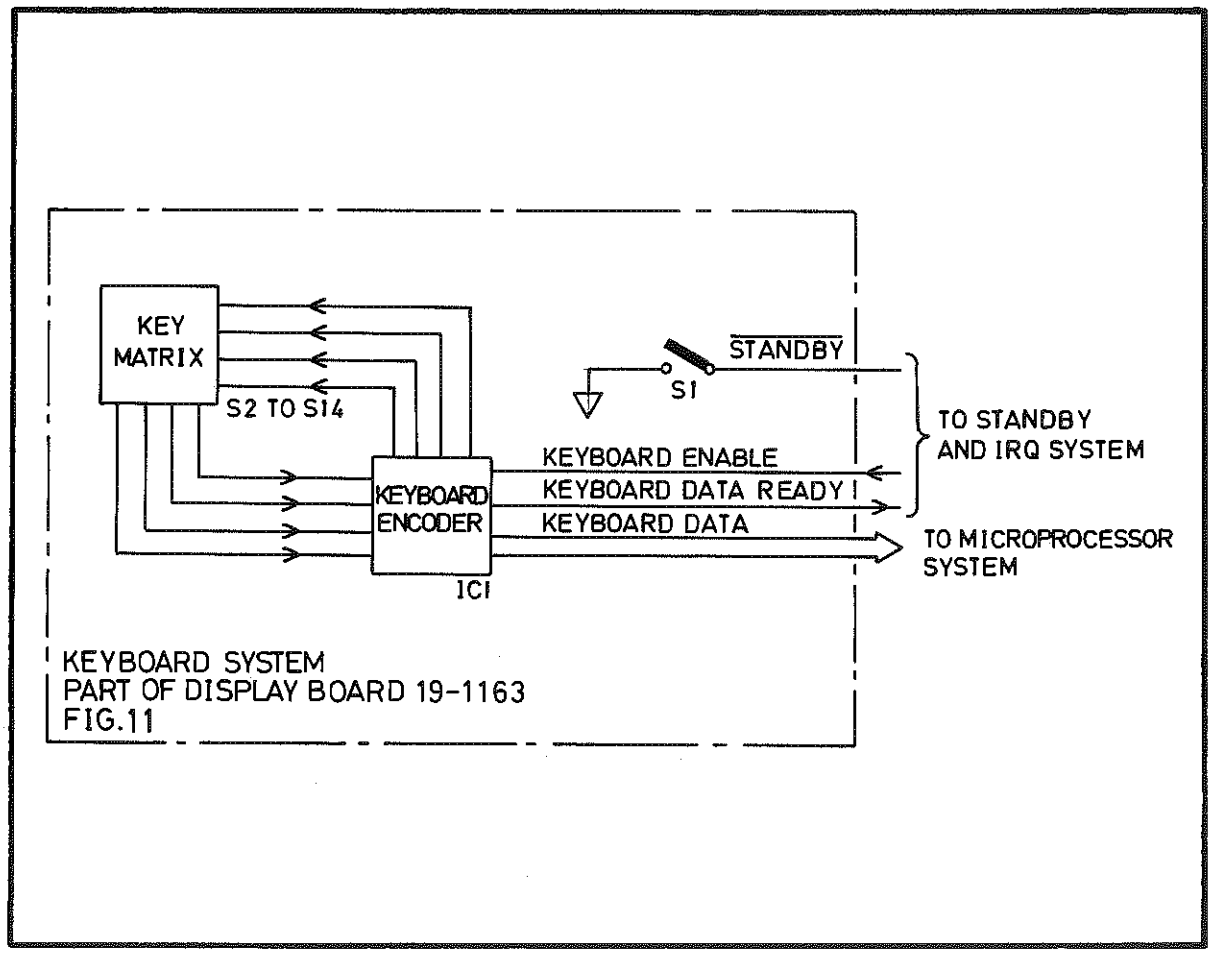


Fig 6.8 The Keyboard System

Circuit Description

74 The circuit diagram is given in Fig 11 in Section 8. The keys are arranged in a 4 x 4 matrix having row lines connected to the encoder at IC1/7, 8, 10 and 11. The column lines are connected to IC1/1, 2, 3 and 4.

75 The encoder normally holds the row lines at logic '0'. When a key is pressed the corresponding column line is pulled to logic '0'. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register.

76 When the key-position code has been stored, the encoder sets the KEYBOARD DATA READY line, at SK2 pin 4, to logic '1' giving a microprocessor interrupt. The microprocessor sets IC1/13 to logic '0', using the KEYBOARD ENABLE line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code to find which key has been pressed.

THE MICROPROCESSOR SYSTEM

Function Description

77 A block diagram of the system is given in Fig 6.9. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

78 Two latches, fed from port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. A buffer is used to read the status of the instrument flags via port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement system, and are controlled by the $\overline{\text{MCC SELECT}}$ signal. The display data latches are in the display system, and are controlled by strobe and chip select signals obtained from port A.

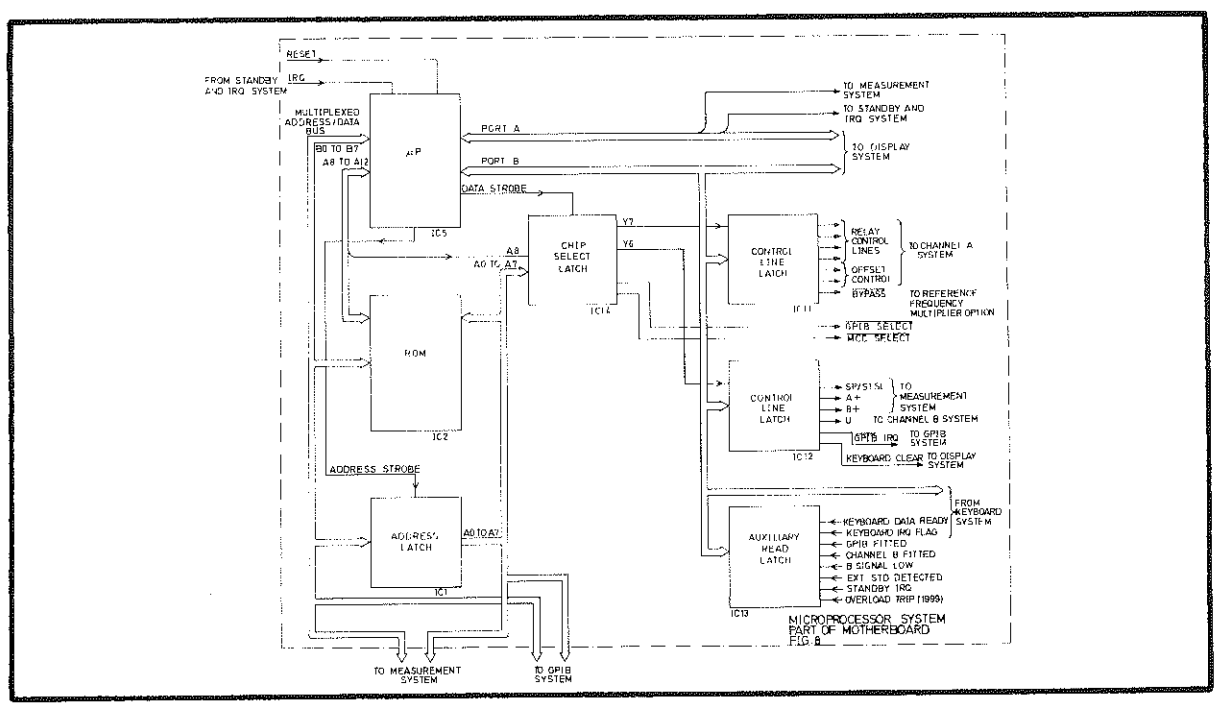


Fig 6.9 The Microprocessor System

Circuit Description

79 The circuit diagram is given in Fig 8 in Section 8. The microprocessor clock and timer signals are generated in the measurement system, and are fed to IC5/39 and IC5/37. A $\overline{\text{RESET}}$ signal is generated in the standby and IRQ system when the instrument is switched on or off, and is fed to IC5/1.

80 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data, is designated B0 to B7. The microprocessor also has two input/output ports, PA0 to PA7 and PB0 to PB7.

Multiplexed Bus Operation

81 The microprocessor puts IC5/6 (ADDRESS STROBE) to logic '1' and IC5/4 (DATA STROBE) to logic '0'. This enables the address latch, IC1 (IC1/11 at logic '1') disables the ROM, IC2 (IC2/20 at logic '1') and disables the address decoder, IC14 (IC14/6 at logic '0').

82 The address is put onto lines B0 to B7 and A8 to A12. When the lines have settled the ADDRESS STROBE line is taken to logic '0'. The low-order bits of the address are latched into IC1, and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

Address Decoding

83 The levels on address lines A6 to A12 are decoded in IC14 to provide the following outputs:

(1) $\overline{\text{MCC SEL}}$, the chip-select signal for IC9.

(2) $\overline{\text{GPIB SEL}}$, the chip-select signal for the GPIB address decoder.

(3) Y6, the chip-select signal for output latch IC12.

(4) Y7, the chip-select signal for output latch IC11.

84 These outputs are only available when IC14 is enabled by a logic '1' at IC14/6 and a logic '0' at IC14/4 and 5. The level at IC14/6 is set by the DATA STROBE output at IC5/4, which is at logic '1' when the multiplexed bus is available for data transfer. All outputs from IC14 are decoded from addresses with lines A9 to A12 at logic '0', when IC14/4 and 5 are held at logic '0' by the output from IC3a, b and d.

Input and Output Latches

85 The logic levels required on the instrument control lines are set into the output latches, IC11 and IC12, from data port B of the microprocessor. The latch strobe signals are decoded in IC14. Data may be read by the microprocessor from the input latch, IC13. The latch strobe signal is provided via data port A of the microprocessor.

THE STANDBY AND IRQ SYSTEM

Functional Description

86 The system generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement system and the keyboard system for connection to the microprocessor. A block diagram is given in Fig 6.10.

87 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

88 On switching to standby, the $\overline{\text{STANDBY}}$ signal from the keyboard system sets the standby IRQ latch. The latch outputs provide the standby IRQ and a standby flag for the microprocessor system. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY indicator and disable IC7b, so inhibiting the other IRQs. At the end of the microprocessor interrupt routine the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

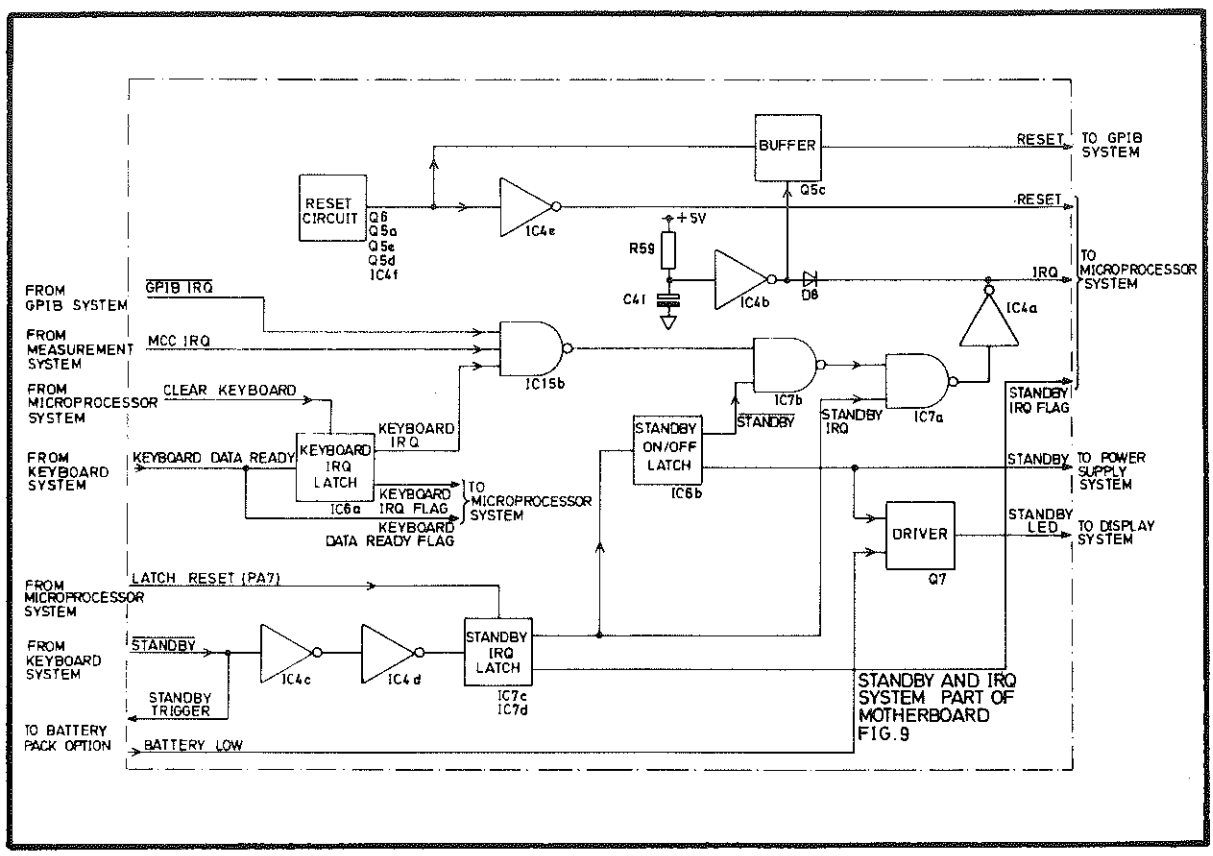


Fig 6.10 The Standby and IRQ System

89 While the instrument is in standby, the input to IC4b is held low and the IRQ input to the microprocessor is held high via D8. This inhibits all IRQs. The output from IC4b also holds the GPIB interface reset via Q5c.

90 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard system. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation and IC7b is enabled. The input to IC4b rises as C41 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC7a. At the end of the restart sequence the standby IRQ latch is reset.

91 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

Circuit Description

92 The circuit diagram is shown in Fig 8 in Section 8.

Reset Circuit

93 The $\overline{\text{RESET}}$ signal is generated in the circuit containing Q6, Q5a, d and e, and C40. When the instrument is switched on, the input to IC4f is held low until C40 charges through R46, Q5a and R55. The output at IC4f/12 goes to logic '1' when power is applied, but drops to logic '0' after approximately 300 ms. This output is inverted by IC4e to provide the microprocessor reset and by Q5c to provide the GPIB reset.

94 If there is a reduction in the +5 V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R47 falls. The potential at Q6 emitter is maintained by the charge in C40, so Q6 conducts. The current in R52 makes the base of Q5d positive, so the transistor conducts and holds the base of Q6 low until C40 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

Standby Operation

95 On switching to standby, PL1 pin 14 is taken to 0 V by the STANDBY key. Debouncing is provided by R50 and C37. The leading edge of the signal is sharpened in IC4c, C38, R51 and IC4d, and sets the standby IRQ latch, IC7c and d.

96 The negative-going output from IC7c/10 is passed via IC7a, IC4a and R58 to IC5/2, to provide a microprocessor interrupt. The positive-going output from IC7d/11 forms the standby IRQ flag (read by the microprocessor via IC13 during the interrupt routine) and clocks the standby latch, IC6b, to the set state.

97 The logic '0' level at IC6b/8 switches on Q7, and provides power for the STANDBY indicator via PL1 pin 8. The same output is applied to IC17b/5, and disables the other interrupts, which are connected to IC17b/6.

98 The logic '1' level at IC6b/9 shuts down the power supplies except the +5 V STANDBY supply.

99 At the end of the interrupt routine the microprocessor resets the standby IRQ latch by applying logic '1' to IC7c/8 from IC5/7.

100 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag, as before. The positive-going output from IC7d/11 clocks the standby latch back to the reset state, so that the STANDBY indicator is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

101 When the instrument is operating from the battery pack in the battery-save mode, the $\overline{\text{STANDBY TRIGGER}}$ control line (PL21 Pin 7 on Fig 7) is taken to logic '0' after approximately one minute by the battery pack. This switches the instrument to the standby mode. The instrument is returned to the measurement mode by operation of the STANDBY key.

The IRQ Circuits

102 The KEYBOARD DATA READY line, at PL2 pin 4, goes to logic '1' when the keyboard encoder has data available. This clocks IC6a to the set state to provide a keyboard IRQ flag at IC13/11 and an interrupt signal at IC15b/9. Interrupts from the measurement system ($\overline{\text{MCC IRQ}}$) and the GPIB interface ($\overline{\text{GPIB IRQ}}$) are connected to IC15b/12 and IC15b/10 and 13.

103 If any of these interrupts occurs, IC15b/8 and IC7b/6 will go to logic '1'. Provided the standby latch, IC6b, is not set, IC7b/5 will be at logic '1' and the interrupt signal passes via IC7a and IC4a to IC5/2.

104 When the instrument is switched into or out of the standby state, the standby IRQ latch, IC7c and d, is set. The standby IRQ from IC7c/10 is fed to IC5/2 via IC7a and IC4a.

105 The circuit comprising R59, C41, IC4b and D8 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q5c) while the +5 V power supply to R59 is switched off. On return from standby, C41 charges and IC4b/4 goes to logic '0'. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ which occurs on return from standby from being acted upon before the power supplies are fully restored.

THE POWER SUPPLY SYSTEM

Functional Description

106 A block diagram of the system is given in Fig 6.11. The AC supply enters at a plug mounted on the rear panel, and passes via a fuse and RFI filter, mounted on the motherboard, to the line switch.

107 The switched supply is connected to the primary winding of the power transformer via the operating voltage range selector. This has the form of a plug-in printed circuit board, which is positioned according to the line voltage.

108 The transformer has a tapped secondary winding, which supplies two rectifiers.

109 The rectifiers feed regulators providing +11.2 V, +5 V, +5 V and -5.2 V. Alternatively the raw supplies can be supplied by the Battery Pack Option, if fitted. The -5.2 V regulator and one of the +5 V regulators, which supply most of the instrument's circuits, are shut down by a signal from the microprocessor system when the instrument is switched to standby.

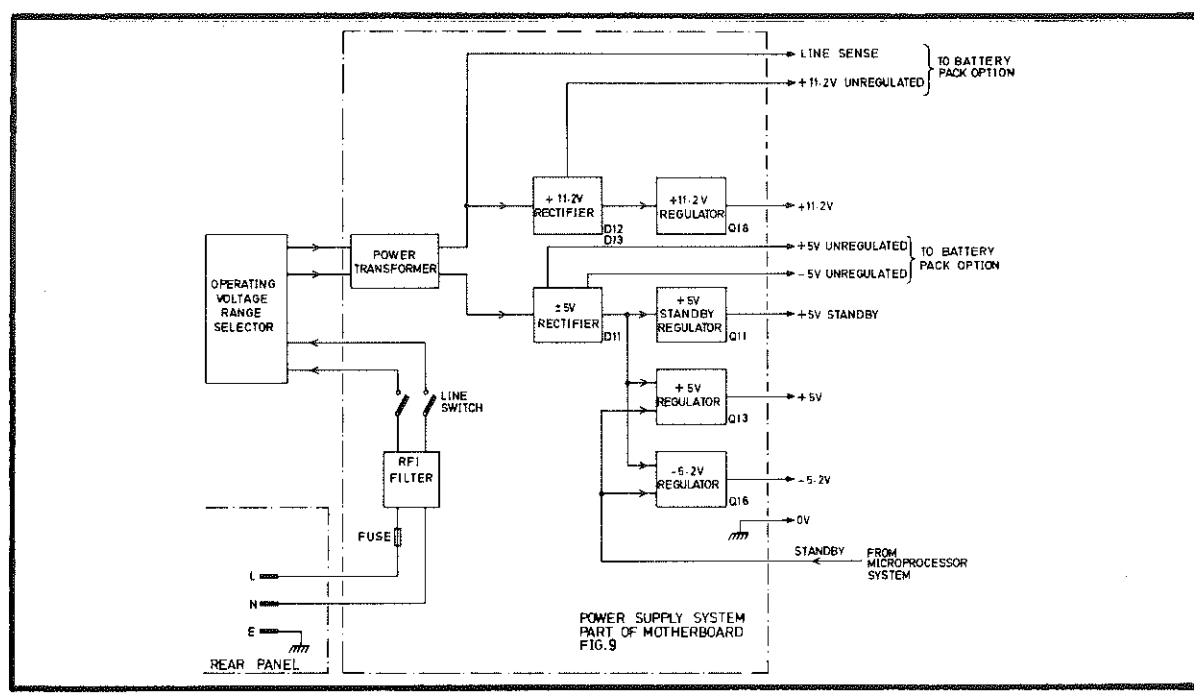


Fig 6.11 The Power Supply System

Circuit Description

110 The circuit diagram is shown in Fig 9 in Section 8. AC power connected at the power input plug passes via fuse FS1 and the RF filter, formed by L10, L11, C47, C49 and C50, to the POWER switch, S1b. The switched supply is connected to the primary windings of T1 via the tracks of a printed circuit board, which is inserted in SK8.

111 The secondary windings of T1 supply the ± 5 V rectifier, D11, C58 and C59, and the +11 V rectifier, D12, D13 and C57. When the instrument is operated from the battery pack, the unregulated supply is fed in via PL21.

112 Separate discrete-component regulators are provided for each supply rail. These are similar in construction, having series regulator elements (Q18, Q11, Q13 and Q16) and integrated circuit error amplifiers (IC8d, c, a and b). The reference voltage for the +11.2 V regulator and the two +5 V regulators is provided by zener diode D15. The reference voltage for the -5.2 V regulator is 0 V.

Standby Mode

113 When the instrument is switched to standby, the standby latch, IC6b on Fig 8, is clocked to the set state. The base of Q9 is pulled high, and IC8a/3 is pulled low. The base of Q14 is pulled low by IC8a, the base current of Q13 is cut off and the regulator is shut down. When the voltage of the +5 V rail falls IC8b/6 goes more negative. The base of Q15 is taken towards 0 V by IC8b, so that the base current of Q16 is cut off and the -5.2 V regulator is shut down.

THE FREQUENCY STANDARD SYSTEM

Functional Description

114 The internal frequency standards 19-1147 and 19-1208 are 10 MHz oscillators. Frequency standards 9423 and 9444 each comprise a 5 MHz oscillator and a frequency doubler. A block diagram of the 9423 and 9444 oscillators is shown in Fig 6.12.

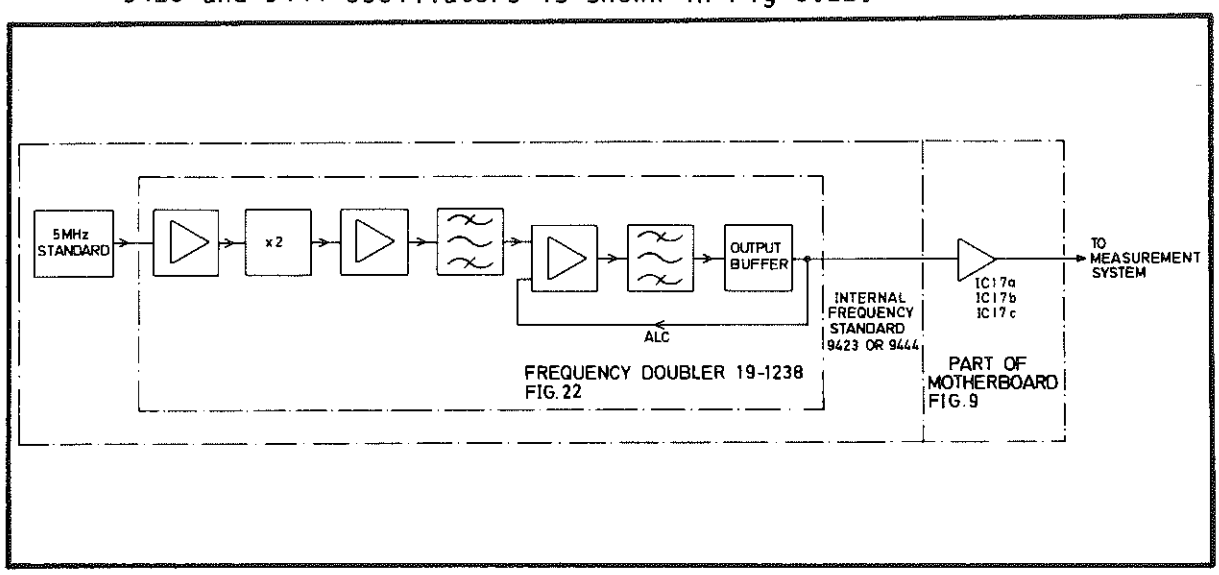


Fig 6.12 9423 and 9444 Oscillators

115 For all oscillator types the 10 MHz signal is passed to the measurement system via a buffer on the motherboard.

116 Signals from an external frequency standard are applied to a signal conditioning circuit on the motherboard. If a 10 MHz external frequency standard is used, the output of this circuit may be connected directly to the measurement system. For external frequency standards at sub-multiples of 10 MHz, the external frequency multiplier option is fitted between the conditioning circuit and the measurement system.

Circuit Description

Frequency Doubler

117 The circuit diagram of the frequency doubler, used with frequency standards 9423 and 9444, is given in Fig 22 in Section 8. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier, via D1 and D2, so that the frequency here is 10 MHz.

118 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 via the buffer, Q6.

119 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3, which charges via R12 and discharges via Q4. If the output signal increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

Internal Frequency Standard Buffer

120 The buffer circuit is shown in Fig 9 in Section 8. The 10 MHz input at PL14 pin 4 is shaped and buffered in IC17a, IC17c and IC17b before being fed to the measurement system at IC18/2. The inverting inputs of IC17 are connected to the bias voltage at IC17/11.

External Frequency Standard Buffer

121 The buffer circuit is shown in Fig 9 in Section 8. The signal connected to the EXT. STD. INPUT socket on the rear panel is fed to PL20 pin 4. Protection against excessive signal amplitude is provided by D9, D10 and R68.

122 The buffer comprises IC16c, IC16a and IC16b. The inverting inputs of IC16c and IC16a are connected to the bias voltage at IC16/11. The final stage has feedback connected via R77 to give a Schmitt trigger action.

123 The differential output of the final stage is fed to PL16 pins 6 and 9 for use in the reference frequency multiplier option. If the option is not fitted, PL16 has LK5 fitted between pins 5 and 6 and LK6 between pins 8 and 9 to connect the signals to the measurement system at IC18 pins 3, 15 and 16.

THE REFERENCE FREQUENCY MULTIPLIER (OPTION 10)

Functional Description

124 The block diagram of the multiplier is given in Fig 6.13. The input to the circuit is taken from the EXT STD INPUT socket on the rear panel, via a signal conditioning circuit on the motherboard. The output of the circuit is passed to the measurement system. The $\overline{\text{BYPASS}}$ control line is held at logic '1' by the microprocessor when the external standard is in use. When the RATIO A/D measurement function is selected the EXT STD INPUT socket is used as the channel D input. The $\overline{\text{BYPASS}}$ control line is then held at logic '0', the switching signal generator is disabled, and the channel D signal is connected directly to the measuring system via the bypass logic.

125 The circuit contains a 10 MHz oscillator operating in a phase-locked loop. If an external reference signal of suitable amplitude is present at the EXT. STD. (D) INPUT socket, a rectangular waveform at the reference frequency is fed to the external reference detector. The detector output triggers the switching signal genertor. The oscillator is then enabled and the bypass logic connects the 10 MHz from the buffer and splitter to the output.

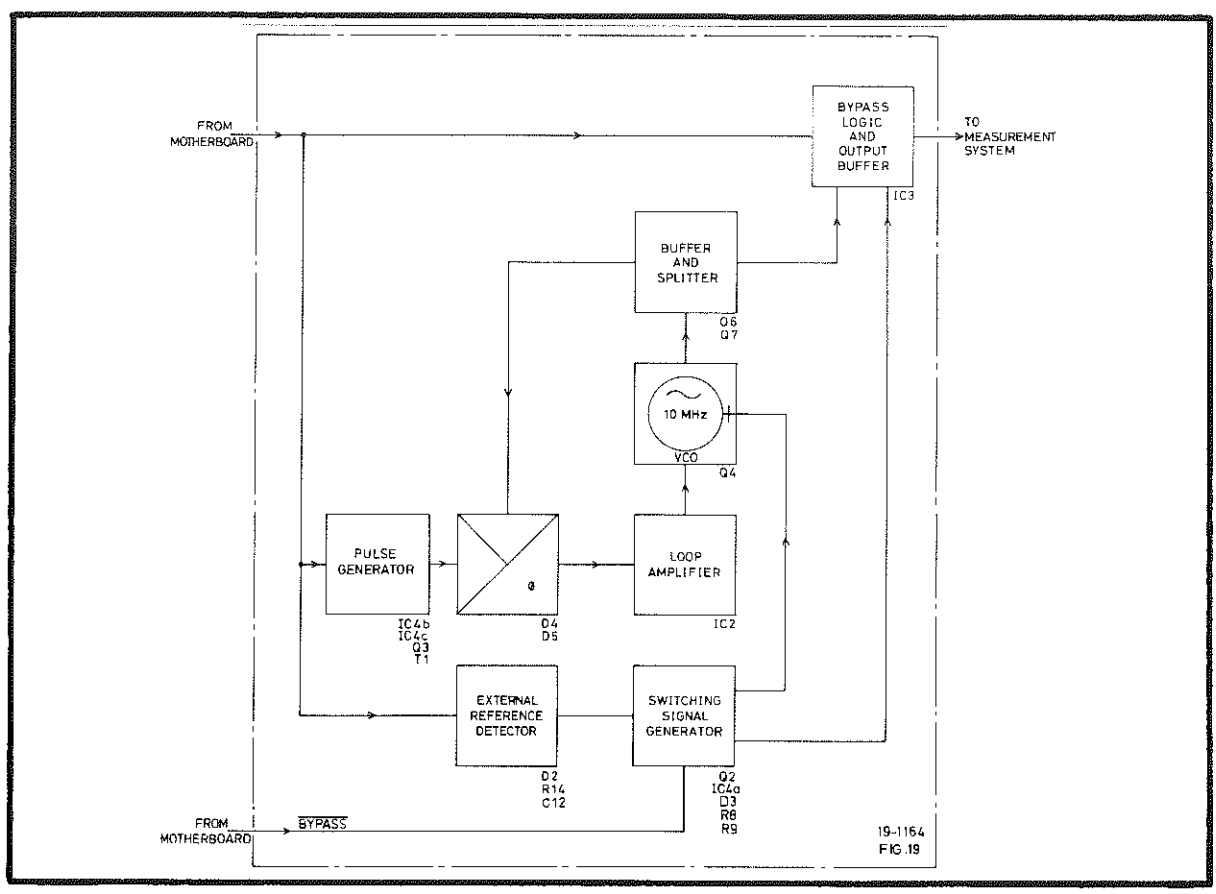


Fig 6.13 The Reference Frequency Multiplier

126 The pulse generator output is fed to the phase detector, and forms the reference signal for the phase-locked loop. The phase detector is of the sampling type, allowing the oscillator to be phase-locked to a reference signal of 10 MHz or any sub-multiple of 10 MHz.

127 If no external reference signal of suitable amplitude is present at the EXT. STD. (D) INPUT socket, the reference detector output does not trigger the switching signal generator. The oscillator is disabled and the bypass logic connects the circuit input to the output.

Circuit Description

128 The circuit diagram is given in Fig 19 in Section 8.

Input Circuit and Pulse Generator

129 Two antiphase waveforms derived from the external reference signal enter the system at SK16 pins 6 and 9. The waveform from pin 9 is converted from ECL to TTL levels in Q1 and squared in IC4d before being applied to the pulse genertor, IC4b and IC4c. The operation of this circuit is illustrated in Fig 6.14.

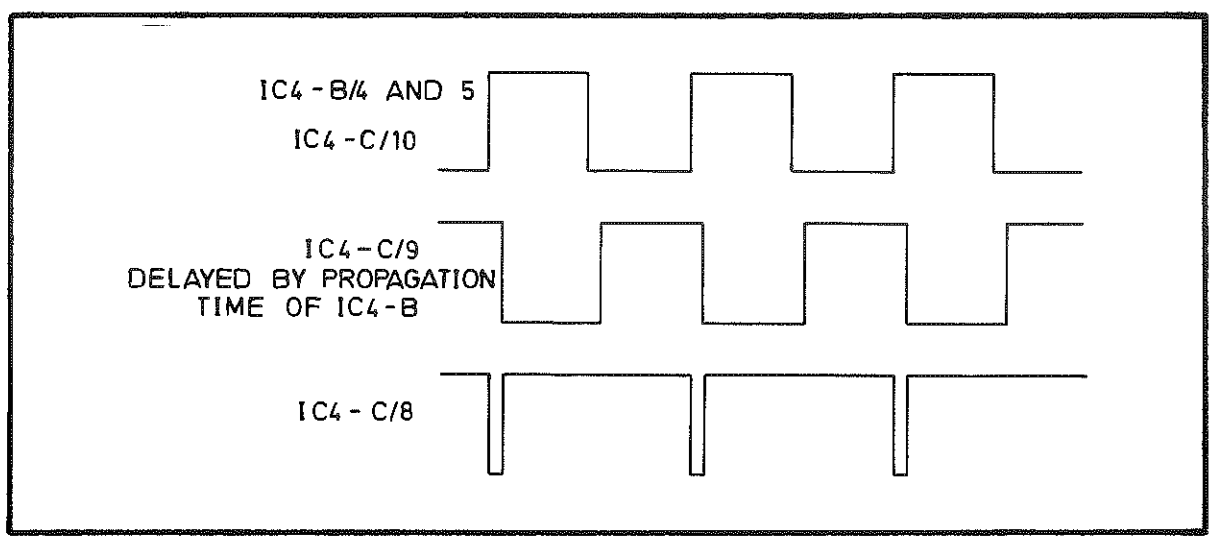


Fig 6.14 Pulse Generator Waveforms

130 The negative-going pulses at IC4c/8 are used to switch Q3, which drives the transmission-line type transformer, T1. The transformer acts as a phase splitter, so that, for the duration of each pulse from IC4c/8, the sampling bridge of the phase detector is held forward biased, with the D4A/D5A and D4B/D5B junctions symmetrical about 0 V.

The Phase-Locked Loop

131 The loop oscillator active element is Q4. The oscillator frequency is controlled by the crystal XL1 and the varactor diode D1. The trimming capacitor C2 can be adjusted to compensate for a range of crystal and varactor tolerances.

132 The oscillator output drives a unity-gain cascode buffer, Q6/Q7. The buffered signal from the collector of Q7 forms the RF input to the phase detector.

133 When the sampling bridge of the phase detector is forward biased by the pulses from T1, the D5A/D5B junction adopts the same potential as the D4A/D4B junction. At other times the junctions are isolated from each other by the high impedance of the non-conducting diodes. The bridge output is therefore a series of samples of the loop oscillator waveform, taken at the frequency of the external frequency standard.

134 The phase detector output depends upon the relative frequency of the loop oscillator and the frequency standard, and upon the phase of the loop oscillator waveform at the instant of sampling. If the standard frequency is 10 MHz every cycle of the loop oscillator output is sampled, but if it is a sub-multiple of 10 MHz only every second, fourth, fifth or tenth cycle will be sampled. In all cases, however, provided the standard frequency is an exact sub-multiple of the loop oscillator frequency, the samples will be of constant amplitude. If the standard frequency is not an exact sub-multiple of the loop oscillator frequency the output pulses will be amplitude modulated.

135 The amplitude of each phase detector output pulse depends upon the instantaneous value of the loop oscillator waveform at the instant of sampling. The pulses are integrated in C7 to form the input to the loop amplifier IC2. When the loop is in lock the voltage across C7 maintains the voltage at IC2/6, and therefore across the varactor, at the level needed to maintain the loop oscillator at the lock frequency.

External Reference Detector and Bypass Switching

136 The output from IC4d/11 is fed to a detector formed by D2, C12 and R14. If no external reference signal is present at the EXT. STD. (D) INPUT socket, SK16 pin 9 is held low, Q1 conducts and IC4d/11 is at logic '1'. The detector output, and therefore the base of Q2, is at +5V and Q2 is switched off. A logic '0' level is applied to IC4a/2, giving a logic '1' at IC4a/3 and the base of Q5. The zener diode, D3, converts the logic levels from TTL to the level required to switch Q5. R8 and R9 provide ECL logic levels for IC3b and c.

137 With Q5 switched on the voltage across R4 holds the emitter of Q4 positive with respect to its base, disabling the oscillator. At the same time a logic '1' level taken from the junction of R8 and R9 is applied to IC3b/7 and IC3c/11. This disables IC3c and enables IC3a, so that the oscillator output line is open circuited and SK16 pin 6 is connected to SK16 pin 5 and 8 via IC3a and IC3d.

138 When an external reference signal is present at SK16 pin 9 the output from IC4d/11 is a TTL square waveform at the external reference frequency. The detector output holds the base of Q2 negative, so that Q2 conducts and IC4a/2 is at logic '1'. Since IC4a/1 is held at logic '1' by +5 V at SK17 pin 4, IC4a/3 is at

logic '0'. Under these conditions Q5 is cut off and the loop oscillator is enabled. A logic '0' is applied to IC3b/7 and IC3c/11 from the junction of R8 and R9. This disables IC3a and enables IC3c, so that the oscillator output is connected to SK16 pins 5 and 8 via IC3c and IC3d.

THE GPIB INTERFACE (OPTION 55)

Introduction

139 The GPIB interface is a self-contained, microprocessor controlled system. It handles the transfer of data between its internal memory and the GPIB without involvement of the main instrument microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. The circuit diagram is given in Fig 17 in Section 8.

140 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ system. The clock signal is derived from MCC1, IC18, shown in Fig 8 in Section 8.

141 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both address and data. The low-order address bits are put onto the bus first, and are latched into IC11 by the address strobe. The bus is then free for data use.

142 Data transfer between the microprocessors is initiated by an interrupt, and is controlled by a 3-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

Address Setting and Recognition

143 The microprocessor reads the settings of the address switches in switchbank S1, via its port B inputs, approximately every 1 ms and writes the settings into an address register within the generator purpose interface adapter (GPIA) IC12.

144 When the interface address is set on the bus by the controller, it is recognised by the GPIA by comparison with the contents of the internal address register.

Reading From the Bus

145 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12/27 is at logic '0', giving a logic '1' level at IC18d/11. This puts three of the bilateral switches in IC13 to the conducting state, so completing the RFD line. The logic '0' at IC12/27 also puts the buffers in IC14 and IC15 to the receive condition. Data from the bus enters the GPIA data-in register, and IC12/40 goes to logic '0' to provide an interrupt request to the microprocessor, IC9.

146 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder, IC8, is enabled via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-in register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

147 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

Writing to the Bus

148 When the GPIA is addressed to talk its internal data-out register will normally be empty. Under these conditions IC12/40 goes to logic '0' and provides an interrupt request to the microprocessor.

149 IC17a is in the reset state, giving a logic '1' at IC18d/12. Since IC12/27 is at logic '1' when the GPIA is addressed to talk, IC18d/13 is also at logic '1'. The resulting logic '0' at IC18d/11 open circuits three of the bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic '1' at IC19c/10, and holds IC12/18 at 0 V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

150 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC6c, IC6d, IC7a, IC7b and IC7c, using address lines GA7, 9, 10, 11 and 12. The decoder is addressed using lines GA4, 5 and 6, and gives the GPIA enable signal at IC8/15. The data-out register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

151 Following the data transfer, the microprocessor sets IC17a, using line PB7, to give a logic '0' at IC18d/12. This gives a logic '1' at IC18d/11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, so releasing IC12/18 from 0 V. When the listening device asserts that it is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

152 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17a, using line PB6, giving a logic '1' at IC18d/12, so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

Serial Poll

153 The status byte register of the GPIA is normally updated approximately every 1 ms by the microprocessor. When the interface is addressed to talk following the receipt of the serial poll enable (SPE) message, the GPIA puts the status byte onto the bus without further action by the microprocessor.

154 When the serial poll is completed, the controller sends the serial poll disable (SPD) message, which is detected by IC6a, IC6b, IC7d, IC18a and IC19b. The resulting logic '1' at IC17a/3 clocks IC17a to the reset condition, and gives a logic '1' at IC18d/12.

Data Transfer Between Microprocessors

155 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connection between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

156 For data transfer to the GPIB microprocessor, the instrument microprocessor sets PL4 pin 22 ($\overline{\text{GPIB DATA IRQ}}$) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4d. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5d. The microprocessor reads the IRQ flag via IC5d and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

157 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16a via IC20b. The level set on line 0 of the data bus is transferred to IC16/5, and forms the ready for data (RFD) signal to the instrument microprocessor.

158 The instrument microprocessor enables and addresses IC3 to give an enabling signal to IC5c, reads the RFD signal, puts the first data byte on the bus and re-addresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16b, so that the logic level set at IC16b/12 is transferred to IC16b/9 to form the data valid (DAV) signal to the GPIB microprocessor.

159 The GPIB microprocessor addresses IC8 to give a signal to enable IC5a, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output enable signal for IC1 (via IC20c) and reads the data. A data accepted (DAC) signal is sent via IC2 and the RFD signal is reset. The instrument microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been received.

160 Data transfer from the GPIB microprocessor to the instrument microprocessor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18b and IC4c. The IRQ flag is read by the instrument microprocessor during its interrupt routine, via IC5b (enabled by an output from IC3). The IRQ signal is cancelled by the instrument microprocessor setting data bus line 0 to logic '0' and then addressing IC3 to clock IC17b. The resulting logic '0' at IC17b/9 disables IC18b.

161 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16b and IC5a, the DAV signal via IC16b and IC5c, the DAC signal via IC1 and the data via IC2.

THE BATTERY PACK (OPTION 07)

Functional Description

162 The battery pack option allows the counter to be supplied from a +12 V internal battery pack (part of this option) or from an external DC supply. The output from the option is only partially regulated. Fine regulation is done on the motherboard in the normal way.

163 The option is based on a switch-mode flyback converter. It includes a charging circuit for the internal batteries, a battery condition monitor, and other circuits to maintain the charge and optimise battery life.

Flyback Converter

164 This type of switch-mode DC-DC converter relies for its operation on switching a direct current repeatedly on and off, at high frequency, through the primary of a flyback transformer. The resultant AC from the secondaries is rectified to produce a range of DC levels. Output levels are controlled by feedback to the switching circuit.

165 In the block diagram of the option, shown in Fig 6.15, direct current, from either the internal battery pack or an extenal DC supply, passes through the primary of the flyback transformer and through a transistor switch to ground.

166 Switching occurs at a frequency of approximately 40 kHz. Current is first switched on, allowing the magnetic field around the primary to build up. The current is then switched off and the collapsing field transfers its energy to the secondary windings. Secondary voltages are rectified and filtered to provide ±11.2 V UR, +5 V UR and -5.2 V UR.

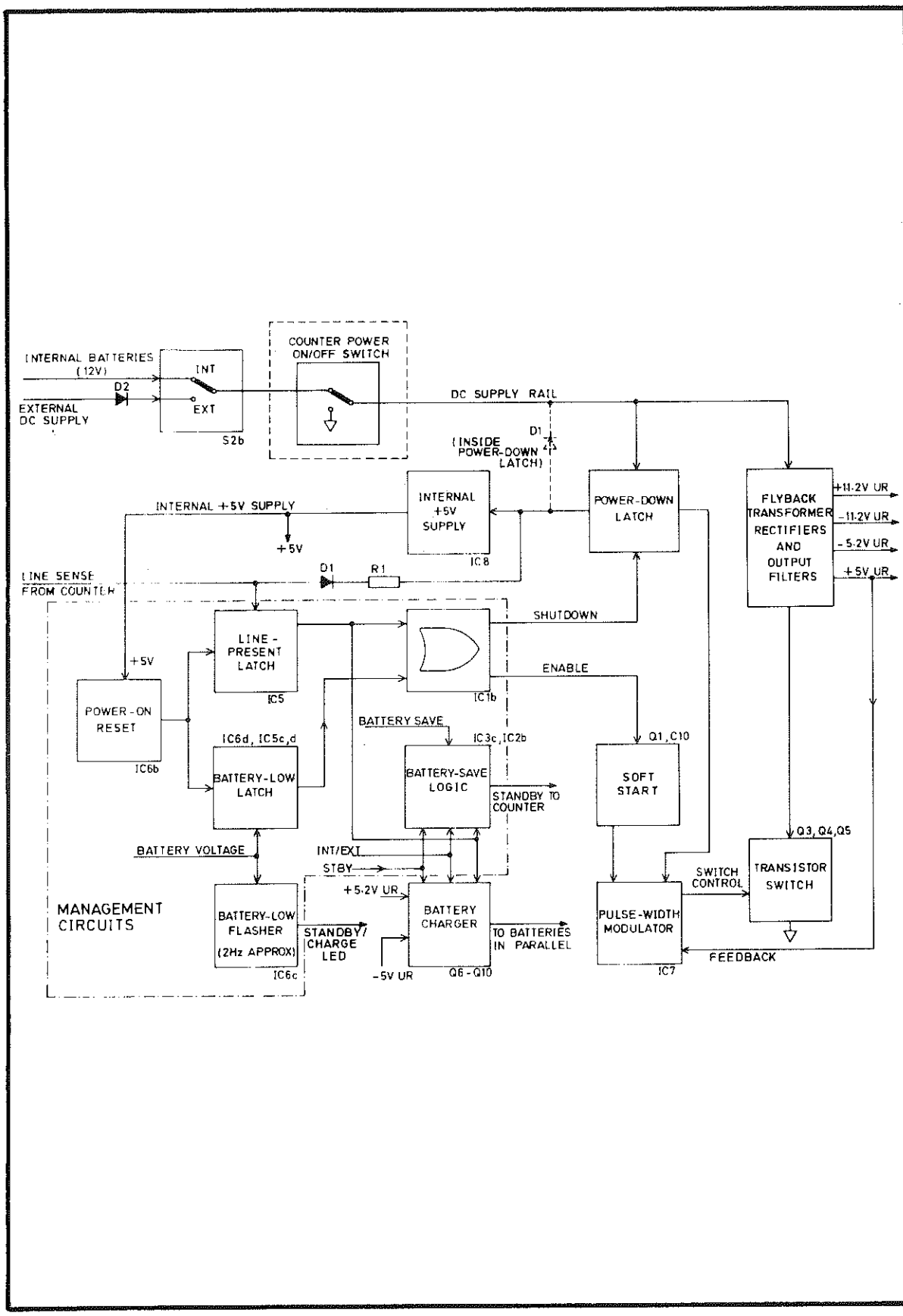


Fig 6.15 The Battery Pack

Feedback

167 For normal loads, the switching duty-cycle is such that the transformer core never has time to saturate, so the power transferred to the secondaries is proportional to the on time of the transistor switch. In the pulse-width modulator, the level of the +5 V output is compared with a reference voltage. If the +5 V is low, the on time of the switch is increased, and if it is high, the on time is reduced. Note that the switching frequency remains constant. Only the duty-cycle is changed.

168 At higher load levels, the duty-cycle is such that the secondary current does not have time to decay to zero between switching pulses. Therefore, the core still retains some energy at the end of the cycle. This means that the next on-time does not have to be increased to provide the extra power. Hence, beyond a certain load current, transistor on-time remains essentially constant. On-time will increase for a few cycles, however, at the instant the load current increases.

169 Feedback is taken from the +5 V UR rail because this has the heaviest load. Each of the other output levels is essentially governed by the ratio of its secondary turns to those of the +5 V UR secondary.

Soft Start

170 At switch-on, the +5 V output would initially be zero. Therefore the feedback circuit just described would create a large current surge. To prevent this, soft start circuitry ensures that the Q5 on pulses are initially very short, and are only gradually increased to normal. Soft start is enabled by a signal from the management circuits.

Power-Down Latch

171 This is essentially an on/off switch for the pulse-width modulator and for a +5 V regulator. It is on when the counter is being powered by the battery pack or an external DC supply. It is switched off when the battery is low (auto-shutdown), and when the counter is being powered from an AC (line) supply.

Management Circuits

172 Control of the battery-pack option, and its response to control switches and to variations of AC or DC supply levels is managed by the management circuits. These are identified in the block diagram.

Line Sense

173 When the counter is being powered from line, an AC signal is available on the line sense input. This is used to operate the line present latch, which disables the pulse-width modulator via the power-down latch.

Battery Low/Auto-Shutdown

174 The battery voltage is monitored by the battery-low latch and the battery-low flasher. If the voltage falls to around +11 V the STBY/CHRG LED on the front panel is flashed at 2 Hz. After approximately 15 minutes' further operation, when the voltage has fallen to around 10.1 V, the battery-low latch will be set and the option will be shut down by the power-down latch.

Battery-Save Facility

175 If the battery-save facility is selected, the battery-save logic will switch the counter into standby mode one minute after it has been enabled.

Internal +5 V Supply

176 The control logic (management circuits) of the option need an independent +5 V supply. This is provided by a +5 V regulator.

177 When the counter is using an AC supply, the regulator is powered by a DC voltage derived from the line sense input. When one of the DC inputs is being used, the regulator is suplied by the DC supply rail via the power-down latch.

Power-On Reset

178 When power is switched on, +5 V is applied to the power-on reset circut. This circuit provides a pulse that resets the line-present and battery-low latches. If there is no AC input on line sense, the power-down latch will be cleared and the soft-start circuit enabled.

Battery Charging

179 The option includes a battery-charger capable of fully-charging a battery-pack within 14 hours, and a trickle-charger designed to top-up a previously charged battery.

Battery Charger

180 This circuit can only be enabled when the counter is powered from the line or from an external DC supply. The charger is powered from the +5 V UR and -5.2 V UR rails, and is enabled by the STBY signal from the STBY/CHRG button.

181 The +12 V battery-pack is formed by two +6 V batteries connected in series. When the charger is enabled, an internal relay configures the two batteries in parallel.

Trickle-Charging

182 Whenever the counter is powered from line, rectifier circuit D1/R1 derives a DC voltage from a 40 V peak-to-peak signal on the line sense input. This supplies approximately +14 V to the DC supply rail via D1 in the power-down latch. If the internal battery is selected, the DC supply rail provides a trickle-charge to top up the battery. Diode D2 prevents the external DC supply from being charged in this way.

Technical Description

183 The circuit of the battery-pack assembly is shown in Fig 23.

Power Sources

184 Option power can be supplied from line, from an external DC supply or from the battery pack.

185 When the counter is powered by line, a 40 V peak-to-peak, 50 Hz signal is applied to LINE SENSE at SK21-15. This is rectified by D1 to produce approximately 14 V DC. The voltage is fed via D1 (in the switch board assembly) to the DC supply rail. In the absence of a line supply the internal battery pack or an external DC supply can be selected at S2.

186 In the EXT position, a DC supply plugged into JK1 is connected via SK21-3 and 4, S1a and SK21 pins 21 and 22, to the DC supply rail.

187 In the INT position of S2, the battery pack is connected to the DC supply rail by the same route.

Switching Circuit

188 Whenever IC7 is enabled, a nominal 40 kHz square wave signal at Pin 9 switches driver transistors Q3 and Q4 on and off in turn. (The totem-pole arrangement provides a fast switching action). This switches MOSFET Q5 on and off in time with the signal on IC7/9. The switching signal is derived from an internal oscillator, the frequency of which is controlled by the value of C13.

Flyback Transformer

189 Each time Q5 is switched off, the field generated around the primary winding collapses, generating a voltage in each of the secondaries. The polarity is such that the points marked with a dot will be negative.

190 The voltages are additive. They are rectified and filtered by D7-D10 and C16-C19 to produce ±11.2 V UR, +5 V UR and -5.2 V UR supplies. These are further regulated on the motherboard.

Level Control

191 A voltage proportional to the +5 V UR level is developed across R30 and connected to the error input (IC7/7) of the pulse-width modulator. The input is compared with the level of an internal reference voltage. The duty cycle of the signal at IC7/9 is modified accordingly.

192 R28 modifies the feedback level, allowing the controlled level to be set precisely.

Soft Start Circuit

193 R26 and C11 form a feedback-loop stability network for the circuit that compares reference and feedback levels. Shunting these components has the same effect as a decrease in the +5 V UR level. This effect is used to produce a soft start at switch-on. The sequence is as follows.

194 When the switch-mode circuits are not operating, a high on IC1b/13 disables IC7 via the power-down latch, and maintains Q1 in the conducting state, holding the base of Q2 at 0 V.

195 When IC1b/13 goes low, IC7 is enabled and Q1 is switched off, allowing C10 to charge via R24.

196 As its base voltage rises, Q2, which will initially conduct heavily, is gradually switched off, allowing IC7/8 to gradually adopt its own level, thus allowing the pulse-width modulator to operate normally.

Power-Down Latch

197 When there is no line supply, the +5 V regulator for the management circuits is powered by the DC supply rail, via the power-down latch. A power-up circuit formed by Q3, R8, R9 and C2, ensures that the latch is always opened at power-up. Once the management circuits are enabled, the latch condition will depend upon the logic signals generated by the management circuits.

198 At power-up, the base of Q3 is held low, switching on Q3 while C2 charges. The voltage developed across R7, switches on Q1, which in turn switches-on Q2, Q4 and Q5.

199 Q2 latches Q1 on by maintaining current through R7 and R4. Thus the circuit remains latched on when C2 is charged and Q3 switched off.

200 Q5 connects the DC supply rail to Vcc on IC7.

201 Q4 connects the DC supply rail to the +5 V regulator IC8, thereby energising the management circuits.

202 Unless the line supply is on, or the DC supply rail is low, the latch will remain open. However, if one of those conditions exists, a high on IC1b/13 will drive the base of Q1 low, and thus break the connection between the DC supply rail, and IC7 and IC8. In this state the current drain on the DC supply rail will be almost nil.

Trickle-Charge Circuit

203 The 40 peak-to-peak line sense signal is rectified by D1/R1. This provides approximately +14 V DC to supply the +5 V regulator, and to trickle-charge the battery-pack (via D1 in the power-down latch).

Full-Charge Circuit

204 The charger circuit is powered by the +5 V UR and -5.2 V UR rails. When the counter is using the line supply, the two rails will be supplied from circuits on the motherboard, otherwise they will be supplied from the switch-mode circuits.

205 It is only possible to enable the charger when a line supply or an external DC supply is being used. When the internal +12 V supply is selected the charger is disabled by a ground on S2a.

206 The charger is enabled when STDBY goes high, generating a high on IC3d/11. This switches on Q6 and the constant current circuit formed by D11, Q7, R34 and RLA.

207 RLA1-RLA4 connect the two +6 V batteries, in parallel, between the -5.2 V UR rail and the cathode of D15.

208 To provide temperature stability, it is necessary to make the charger voltage vary with temperature at a rate of approximately -8 mV/^{o}C. This is done by using the base-emitter junction of Q8 (-2 mV/^{o}C) as a temperature sensor, and then multiplying the sensor voltage by four.

209 The circuit comprising Q8, IC4a, R40, Q9, Q10, D15, R41 and R38 performs the multiplication. IC4a adds the result to a reference voltage from the wiper of R36, which provides adjustment of the charger output voltage, nominally set at +7.63 V at 25^{o}C.

210 The required stable voltage for the reference divider chain R45, R36 and R37 is provided by D13 and R35.

211 Power transistor Q10 provides the current required to charge the batteries. As the charger current passes through R1, a voltage proportional to the current is developed across it. Part of this voltage, tapped across voltage divider R43/R44, is fed back to limit the charging current to 1 A. The feedback voltage, at the inverting input of IC4b, is compared with a fixed voltage developed across reference diode D11. A high voltage across R1 will reduce the base voltage of Q9, thereby reducing the current through Q10 and the batteries.

212 D15 prevents the batteries from becoming discharged due to fault conditions.

Line Sense Circuit

213 The presence of the 40 V peak-to-peak signal is detected by R8, R9, D5, D6, IC5a and IC5b.

214 R8 and R9 attenuate the signal, D5 and D6 limit it to +5 V and 0 V.

215 IC5a and IC5b form the line present latch, which is set by the first rising edge on IC5b/6. Thus providing a high on IC1b/12 and IC3a/1. The line present latch will remain set until the unit is switched off.

Battery Low Indication and Auto-Shutdown

216 Battery voltage is monitored by IC6c via potential divider R10-R13. If the battery drops below approximately 11 V, IC6c will turn on the oscillator formed by IC3b and IC2d. The output of this oscillator (which is high when disabled) is then EXORed with the STBY signal and its output used to flash the STBY/CHRG led at approximately 2 Hz.

217 If the battery falls to below approximately 10.1 V, the output of IC6d (Battery-Down comparator) goes high and sets the battery-low latch (IC5c and d), giving a logic high at IC5c/10. This trips the power-down latch into the off state via IC1b and IC6a, shutting down the converter and reducing battery drain to only leakage currents.

NOTE:
With the internal battery selected, the battery-low indicator will start flashing approximately 15 minutes before the power-down latch disables the unit.

Power-On Reset Circuit

218 At power-up, the non-inverting input of IC6b rises to around 3.3 V. The inverting input, however, is held lower as C6 charges.

219 While its inverting input is low, IC6b/1 is high, clearing the battery-low and line present latches. Once C6 is charged, IC6b/1 will change state, allowing the latches to be controlled by the line-present and battery-low voltages.

Standby/Battery-Save Operation

220 Successive depressions of the STBY/CHRG button operate a bistable circuit on the motherboard. In the set state this puts the counter into standby mode and asserts STDBY at SK21 pin 16. In the clear state, the counter is put into normal operation mode and the STDBY line is at logic '0'. Control of the bistable circuit, and the effect of the STDBY signal, is modified by the NORMAL/BATTERY SAVE and EXTERNAL/INTERNAL switches.

221 When powered from an AC line (IC3a/1 high) or an external battery (IC3a/2 high), the STBY/CHRG button enables and disables the charger as previously described. When STBY is high, SK21 pin 7 is low. This drives the STBY LED, which in this case is used as a charging indicator. $\overline{\text{STBY TRIG}}$ is disabled at IC1a/2.

222 When powered by the internal battery, both inputs to IC3a are low. This disables the charger and removes the disable from IC1a/2. In this case, the STBY/CHRG button is used to enable and disable the standby mode, and the STBY LED is used as a standby indication. The standby function is modified by the state of the NORMAL/BATTERY SAVE switch as follows:

(1) When S1 is in the NORMAL position, $\overline{\text{STBY TRIG}}$ is disabled at IC1a/5. If STDBY is asserted the unit is in standby mode and the STBY LED is on. If STDBY is negated, the unit is in normal operating mode and the STBY LED is off.

(2) When S1 is switched to the BATTERY SAVE position, IC3c/9 and IC1a/5 will go low. If STDBY is in its high sate, these changes will have no effect. However, if STDBY is low or is subsequently toggled to its low state, IC1a/3 will go low and IC3c/10 will go high.

(3) C2 transfers this high to IC2b/5, causing a high on IC2b/4. This has no effect on IC1a/4, which is clamped to +5 V by D3.

(4) As C2 charges, the current through R6 will fall exponentially until, after approximately 1 minute, IC2b/5 will fall below threshold level, taking IC1a/4 low.

(5) With all its inputs low, IC1a asserts $\overline{\text{STBY TRIG}}$, which toggles the standby bistable on the main unit (hence the STDBY signal), putting the counter into standby mode and lighting the STBY LED.

(6) Subsequent operation of the STBY/CHRG button will put the counter back into the normal operating mode and initiate another one-minute cycle.

SECTION 7 MAINTENANCE

INTRODUCTION

1 This section is written in six parts, which relate to:

(1) Test equipment required.

(2) Dismantling and reassembly.

(3) Special functions for diagnostic purposes.

(4) Fault finding.

(5) Setting up instructions for use after repair, or if the instrument fails the overall performance verification.

(6) Overall performance verification procedure.

TEST EQUIPMENT REQUIRED

2 A complete list of the test equipment required to carry out the procedures described in this section is given in Table 7.1. The items required for each operation are listed at the start of the relevant instructions.

3 A particular model of test equipment is recommended in some cases, but other equipment having the required parameters given in Table 7.1 may be used. Although the procedures to be followed are given in general terms, they are based on the use of the recommended test equipment. Some modification to the procedure may be necessary if other test equipment is used.

DISMANTLING AND REASSEMBLY

Introduction

4 Instructions for dismantling and reassembling the 1998/1999 are limited to those areas where special care is needed or difficulty may be experienced.

WARNING: LETHAL VOLTAGE
DANGEROUS AC VOLTAGES ARE EXPOSED WHEN THE INSTRUMENT IS CONNECTED TO THE AC SUPPLY WITH THE COVERS REMOVED. SWITCH THE INSTRUMENT OFF AND DISCONNECT THE SUPPLY SOCKET FROM THE REAR PANEL BEFORE CARRYING OUT ANY DISMANTLING OR REASSEMBLY OPERATION.

TABLE 7.1
Test Equipment Required

Item	Description Recommended Model	Required Parameters
1	Signal Generator Racal-Dana 9087	Low phase noise. Jitter 0.5 ns. Frequency range 10 kHz to 1.3 GHz. Output level 1 mV to 1 V. 10 MHz INT STD OUTPUT.
2	Oscilloscope with X1 Probe and X10 Probe	Bandwidth 50 MHz. Y sensitivity 20 mV/cm.
3	Digital Multimeter Racal Dana 4002A	Frequency range: DC to 10 MHz. Level: 20 mV to 20 V range, 1mV resolution. Test voltage for resistance measurement less than 0.5 V.
4	Frequency Standard Racal-Dana 9475	10 MHz. Accuracy better than ±3 parts in 10^{10}.
5	Audio Oscillator Racal-Dana 9083	Frequency range: 10 Hz to 5 kHz. Level: 30 mV into 50 Ω.
6	Pulse Generator Philips PM5771	To provide a single positive-going pulse with a low level of +0.4 V and a high level of +2.4 V. To provide positive and negative-going pulses of 250 mV at 100 kHz with 10% duty cycle. To be capable of driving a 50 Ω load.
7	Connecting Lead	50 Ω coaxial cable with BNC connectors. Length between 80 cm and 1 m (4 off).
8	T-piece	BNC, 50 Ω.
9	Coaxial Load	BNC, 50 Ω.
10	Attenuator	20 dB, BNC, 50 Ω
11*	GPIB Controller HP-85	
12*	GPIB Analyzer Racal Dana 488	

TABLE 7.1 (continued)

Item	Description Recommended Model	Required Parameters
13	Trimming Tool	
14#	True Reading RMS Milli-voltmeter Racal Dana 9301A	Frequency range 10 kHz to 1.3 GHz 30 mV/-20 dB range.
15#£	Power Supply Racal Dana 9232	Voltage range: 0 to 16 V min. Output current: 2 A min.
16#	50 Ω, Power Splitter HP 11667A	N-type.
17#	Connecting Lead	50 Ω coaxial cable terminated: End 1, 3-way Berg socket, pin 1 conductor, pin 2 screen, pin 3 polarising key. End 2, N type plug.
18#	Connecting Lead	Two screened wires, 0.61 m long, terminated: End 1, test pin (23-3446) and small crocodile clip. Capacitor 10 µF 10 V (-ve to test pin wire 150 mm from end, +ve to crocodile clip and wire). End 2, bared conductors.
19#	Power Meter HP 436A (with power sensor HP 8981A)	Frequency range up to 2.6 GHz minimum. Output up to level 10 mV with 0.5 mV resolution
20#	Signal Generator HP 8340A/41A	Frequency range up to 2.6 GHz minimum. Output level up to 10 mV minimum. 10 MHz standard output.
21#	Attenuator Suhner 6806.01.A	6 dB, N-type, 50 Ω.
22#	Co-axial Adaptor	Type N male to BNC male (2 off).
23£	Multimeter AVO 8 Mk II (2 off)	DC current range: 0 to 2 A minimum.

TABLE 7.1 (continued)

Item	Description Recommended Model	Required Parameters
24£	Test Lead	Red and black leads, 2.1 mm coaxial jack to bare ends. Red lead to coaxial jack centre conductor.
25#	Coaxial Adaptor	Type N male to type N male.

NOTES:

* Only required if instrument is fitted with GPIB option.

\# Only required if instrument is 1999 (in addition to unmarked items).

£ Only required if instrument is fitted with Battery Pack option.

Unmarked = all instruments.

Instrument Covers

5 (1) Disconnect the power input socket from the rear panel.

(2) Remove the two screws securing the rear panel bezel: remove the bezel.

(3) If the handles are fitted, peel off the adhesive trim patch from both handles. Remove the two screws securing each handle: remove the handles and spacers.

(4) Remove the top cover by sliding it to the rear of the instrument.

(5) Remove the bottom cover by sliding it to the rear of the instrument.

6 To replace the covers, follow the reverse of the above procedure. Ensure that the top cover is fitted with the access holes towards the front of the instrument, and that the tongues on the ends of the covers are fitted under the edges of the front panel and rear bezel.

Front Panel

7 (1) Remove the instrument covers.

(2) Remove the clamping collar from the A channel input. A suitable slotted screwdriver is included in the Customer Service Support Kit.

(3) Prise the cap off the SENSITIVITY control knob, and remove the knob and nylon washer using a slotted screwdriver.

(4) Remove the two screws and crinkle washers securing assembly 19-1237 to the front panel.

(5) Remove the two screws securing the front panel to the side frame at both sides of the instrument.

(6) Ease the front panel forward until the display board disconnects from the motherboard at PL1 and PL2.

(7) Disconnect the coaxial lead from the back of the B channel input.

8 To replace the panel, follow the reverse procedure. Pass the POWER switch button through the aperture in the panel and reconnect the B channel amplifier before securing the panel. Ensure that the two spacers locate correctly through the screen of assembly 19-1237, and that the SENSITIVITY potentiometer shaft passes through the hole in the front panel. Replace the SENSITIVITY control knob and cap. Secure assembly 19-1237 to the front panel with two screws and crinkle washers.

Rear Panel

9 (1) Remove the instrument covers.

(2) If a PCB-mounted frequency standard is fitted, remove the screws securing it to the rear panel. Pull the PCB assembly upwards until the board disconnects from the motherboard at PL14.

(3) Remove the two screws securing the rear panel to the side frame at both sides of the instrument.

(4) Ease the panel away from the instrument to disconnect assembly 19-1206 from the motherboard at PL19 and PL20.

(5) If an ovened frequency standard is fitted, disconnect the flying lead from PL14.

(6) Remove the nut and crinkle washer securing the rectifier bridge, D11, to the panel.

(7) Disconnect the green/yellow lead connecting the rear panel stud to the power input plug.

10 To replace the panel follow the reverse of the above procedure.

WARNING: LETHAL VOLTAGE
THE GROUNDING OF EXTERNAL METALWORK OF THE INSTRUMENT DEPENDS UPON THE CONNECTION BETWEEN THE REAR PANEL STUD AND THE POWER INPUT PLUG. ENSURE THAT THE GREEN/YELLOW LEAD IS CORRECTLY CONNECTED DURING REASSEMBLY.

1998 Channel B Amplifier

11 (1) Remove the top cover.

(2) Remove the two screws securing the board to the right-hand side frame.

(3) Pull the board upwards to disconnect it from the motherboard at SK7. This allows access to both sides of the board for servicing.

12 To remove the board completely:

(1) Remove the front panel.

(2) Disconnect the coaxial lead from the back of the B channel input.

13 To replace the amplifier follow the reverse of the above procedure.

1999 Channel B Amplifier

14 (1) Remove the top cover.

(2) Remove the four screws securing the board to the right-hand side frame.

(3) Pull the board upwards to disconnect it from the motherboard at SK7.

15 To remove the board completely:

(1) Remove the front panel.

(2) Disconnect the coaxial lead from the back of the B channel input.

16 To replace the amplifier follow the reverse of the above procedure ensuring the coaxial lead is laid into the front panel corner.

Display Board

17 (1) Remove the instrument covers.

(2) Remove the front panel.

(3) Remove the two screws and the inner hexagonal spacer which secure the display board to the front panel and remove the board.

18 To replace the display board, follow the reverse of the above procedure.

Channel A Amplifier

19 (1) Remove the top cover.

(2) Remove the front panel.

(3) Pull the A channel amplifier upwards to disconnect it from the motherboard at SK23. The rear screen will remain attached to the motherboard.

20 To gain access to the front side of the board:

(1) Remove the nut and washer from the SENSITIVITY potentiometer mounting bush.

(2) Unsolder the four tabs securing the front screen to the board, taking care not to damage the PCB metallization.

(3) Lift the screen clear of the board and potentiometer shaft.

SPECIAL FUNCTIONS FOR DIAGNOSTIC PURPOSES

21 The special functions listed in Table 7.2 are provided for use during maintenance. The functions are used in conjunction with the CHECK mode. They are entered by pressing the key sequences shown in Table 7.2. To return to the CHECK mode (special function 70) press

RESET .

TABLE 7.2

Additional Special Functions

Key Sequence	Function Number	Function
CHECK	70	10 MHz check
CHECK OFFSET	71	LED check
CHECK EXT ARM	72	Measurement of short start TEC count
CHECK RECALL	73	Measurement of long start TEC count
CHECK NULL	74	Measurement of short stop TEC count
CHECK 50 Ω/1 M Ω	75	Measurement of long stop TEC count

Special Function 70

22 Special function 70 is the default state. It provides measurement of the 10 MHz internal frequency standard, and verifies operation of the microprocessor system, MCC1, MCC2 and the TEC.

Special Function 71

23 Special function 71 exercises all the LEDs, except STANDBY, GATE, REM, ADDR and SRQ, at approximately 0.5 Hz. If the GPIB interface is fitted, the REM, ADDR and SRQ indicators light.

Special Functions 72, 73, 74 and 75

24 Special functions 72, 73, 74 and 75 should only be used for diagnostic purposes at an ambient temperature of 23°C ± 2°C.

25 The long counts must be 800 ± 220. The short counts must be in the range (0.5 x long count) $^{+20}_{-40}$. Counts outside these ranges indicate that the TEC has failed.

FAULT FINDING

26 A guide to fault location is given in the flow charts of Fig 7.1 to Fig 7.8. The charts provide a logical procedure for localising the fault to an area of circuit. When using the charts it is essential to begin at the start point in Fig 7.1 or Fig 7.6 and act according to the results of each decision box met in turn. Starting part way through any chart is unlikely to lead to satisfactory fault location.

27 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope	2
Digital Multimeter	3
Coaxial Lead	7
GPIB Controller	11
GPIB Analyzer	12

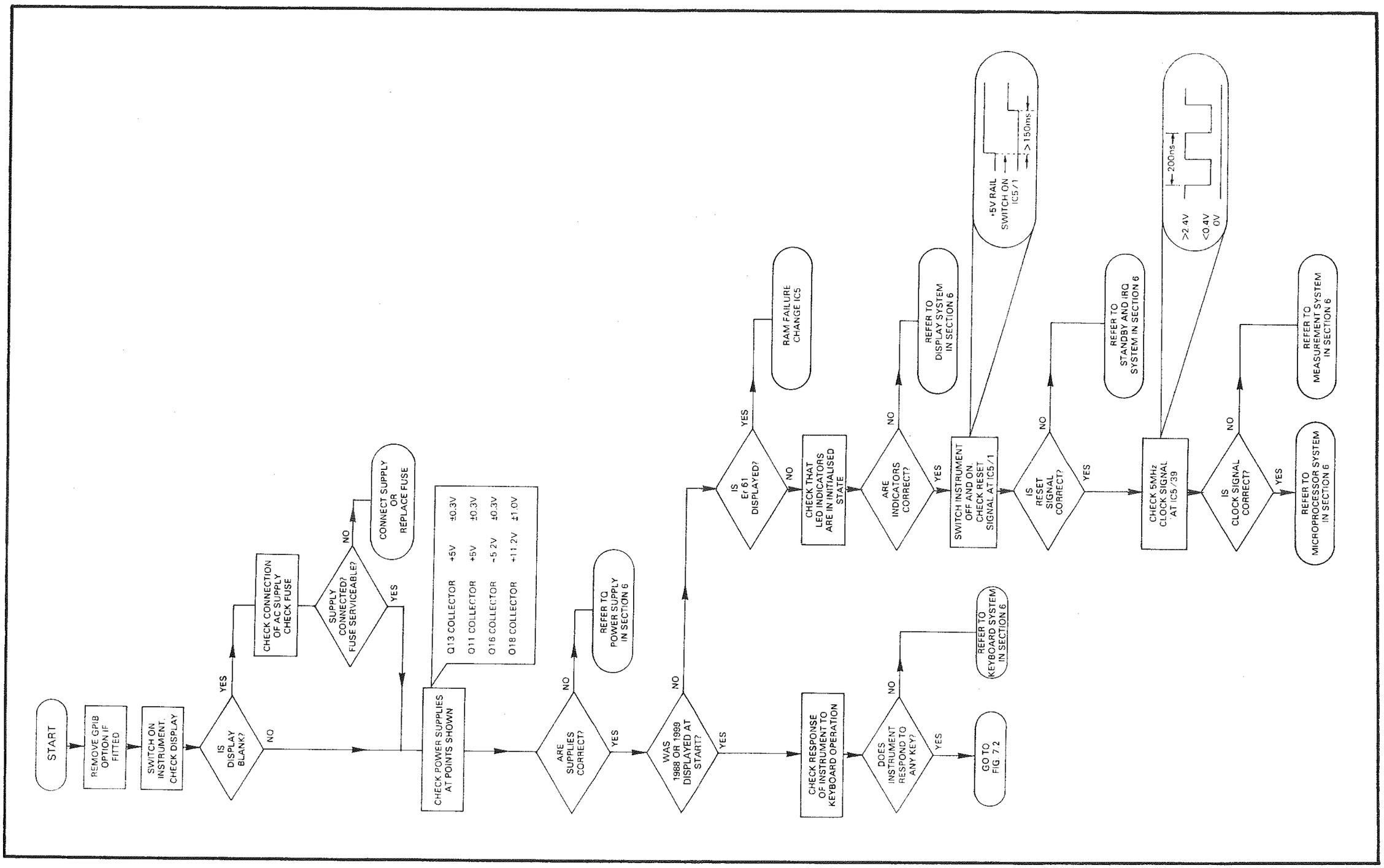


Fig 7.1 Fault Finding Flowchart Part 1

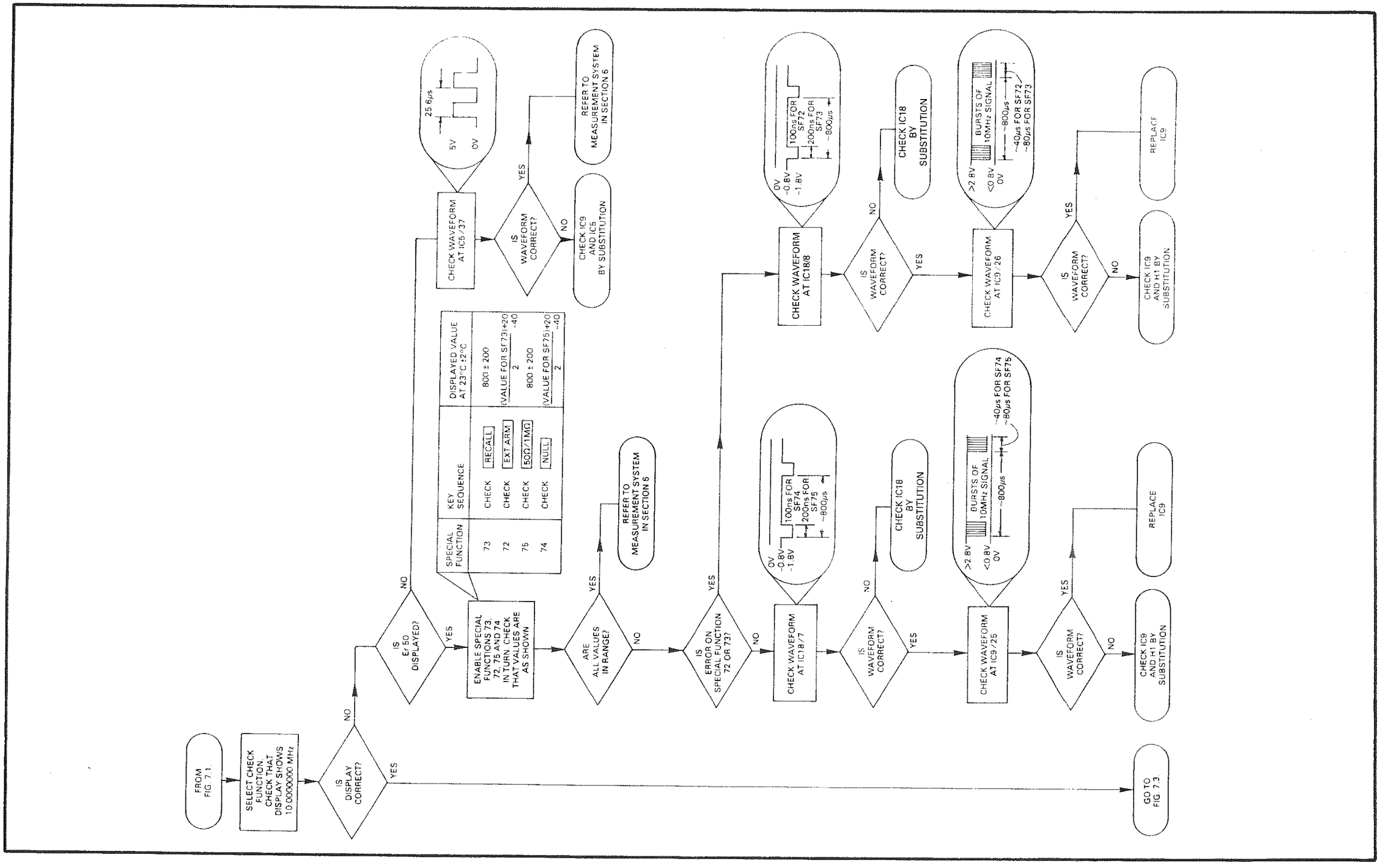


Fig 7.2 Fault Finding Flowchart Part 2

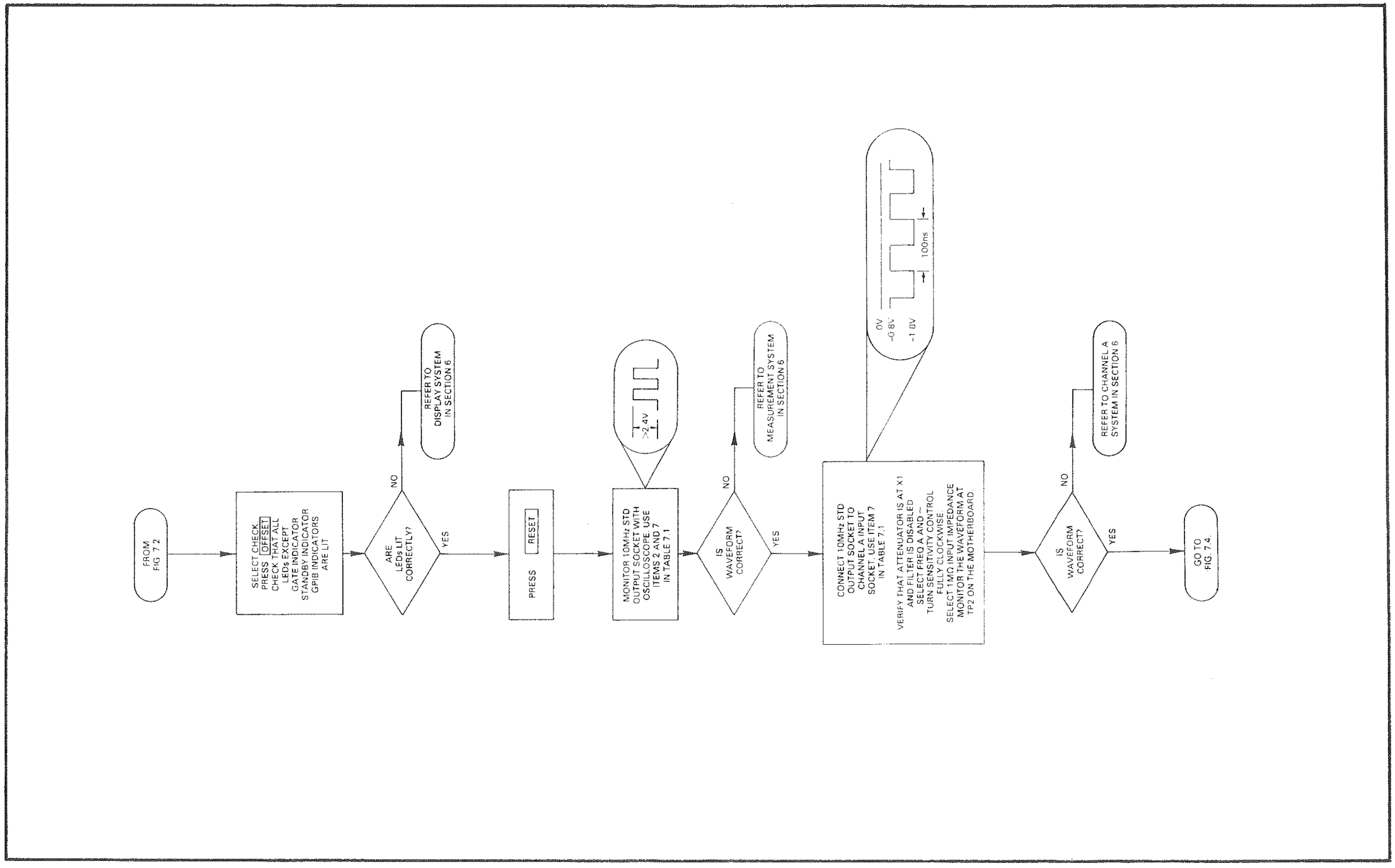


Fig 7.3 Fault Finding Flowchart Part 3

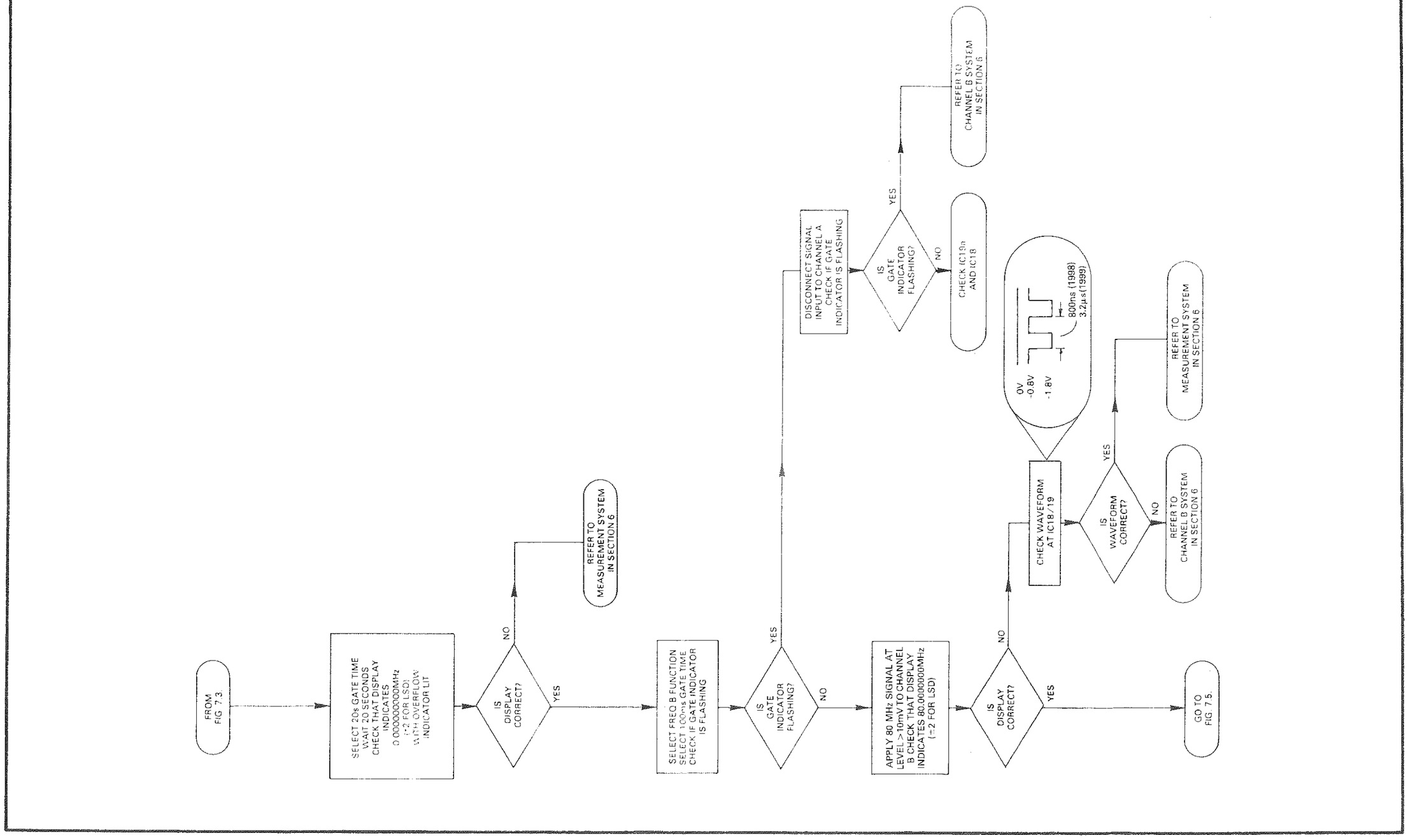


Fig 7.4 Fault Finding Flowchart Part 4

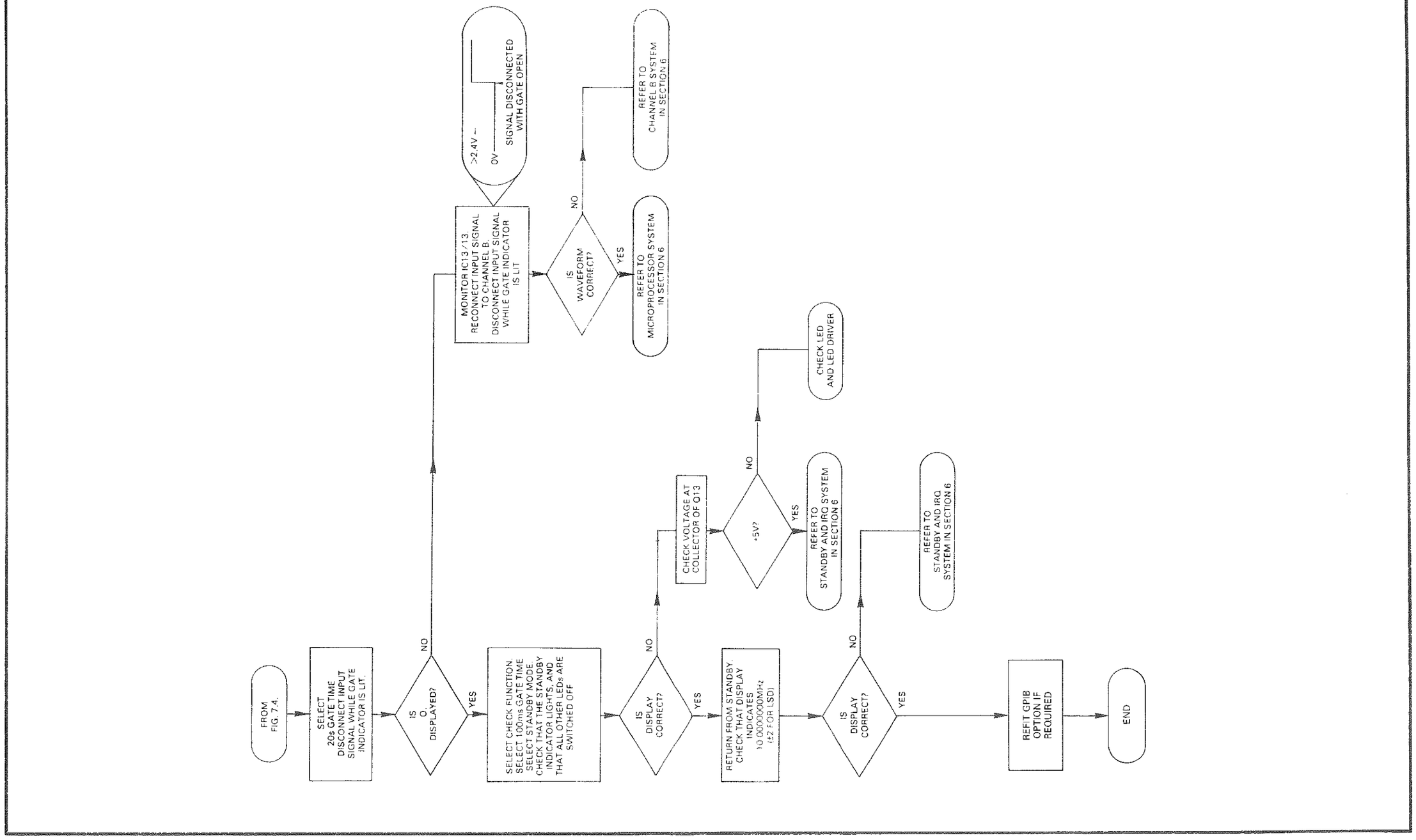


Fig 7.5 Fault Finding Flowchart Part 5

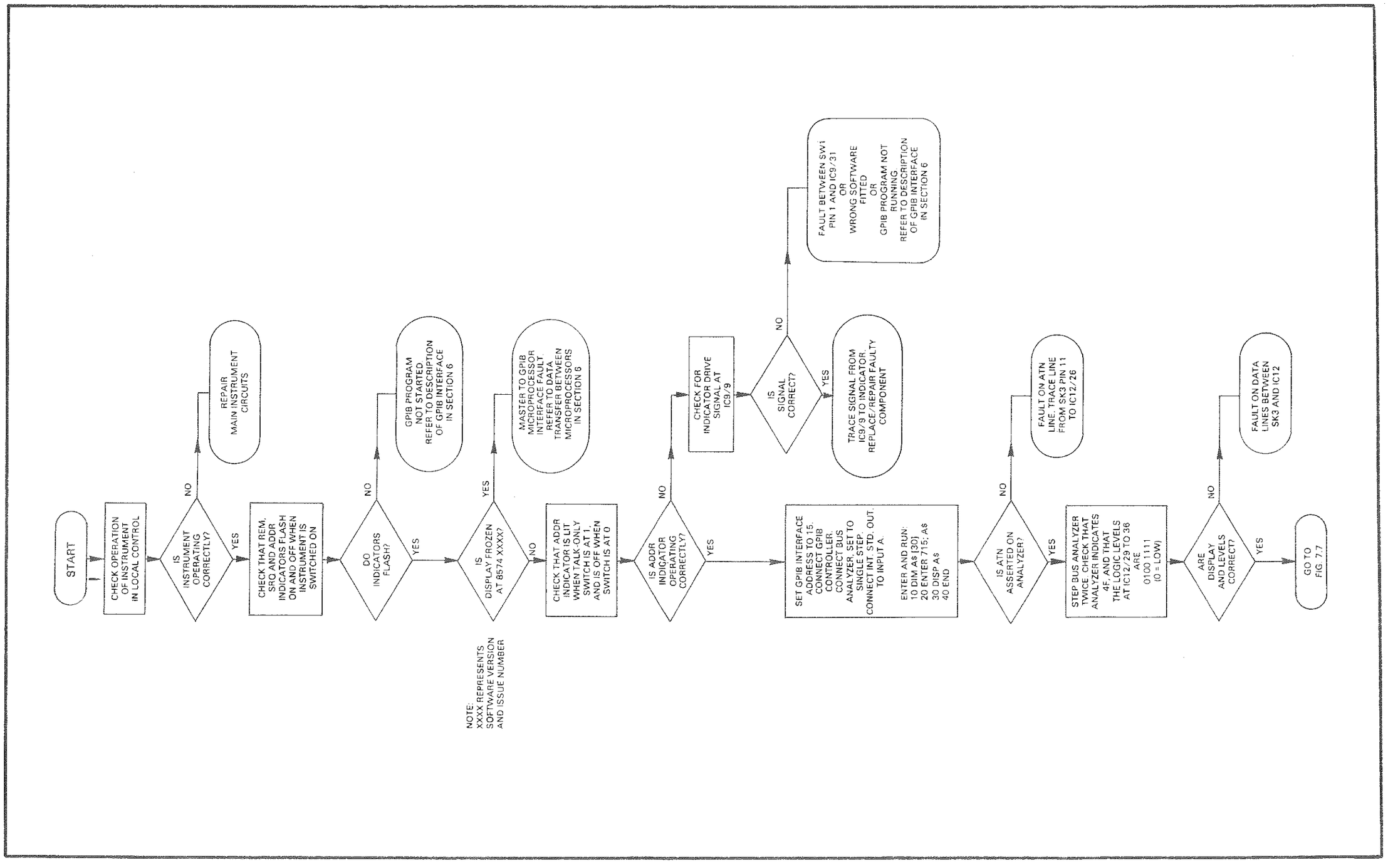


Fig 7.6 Fault Finding Flowchart GPIB Part 1

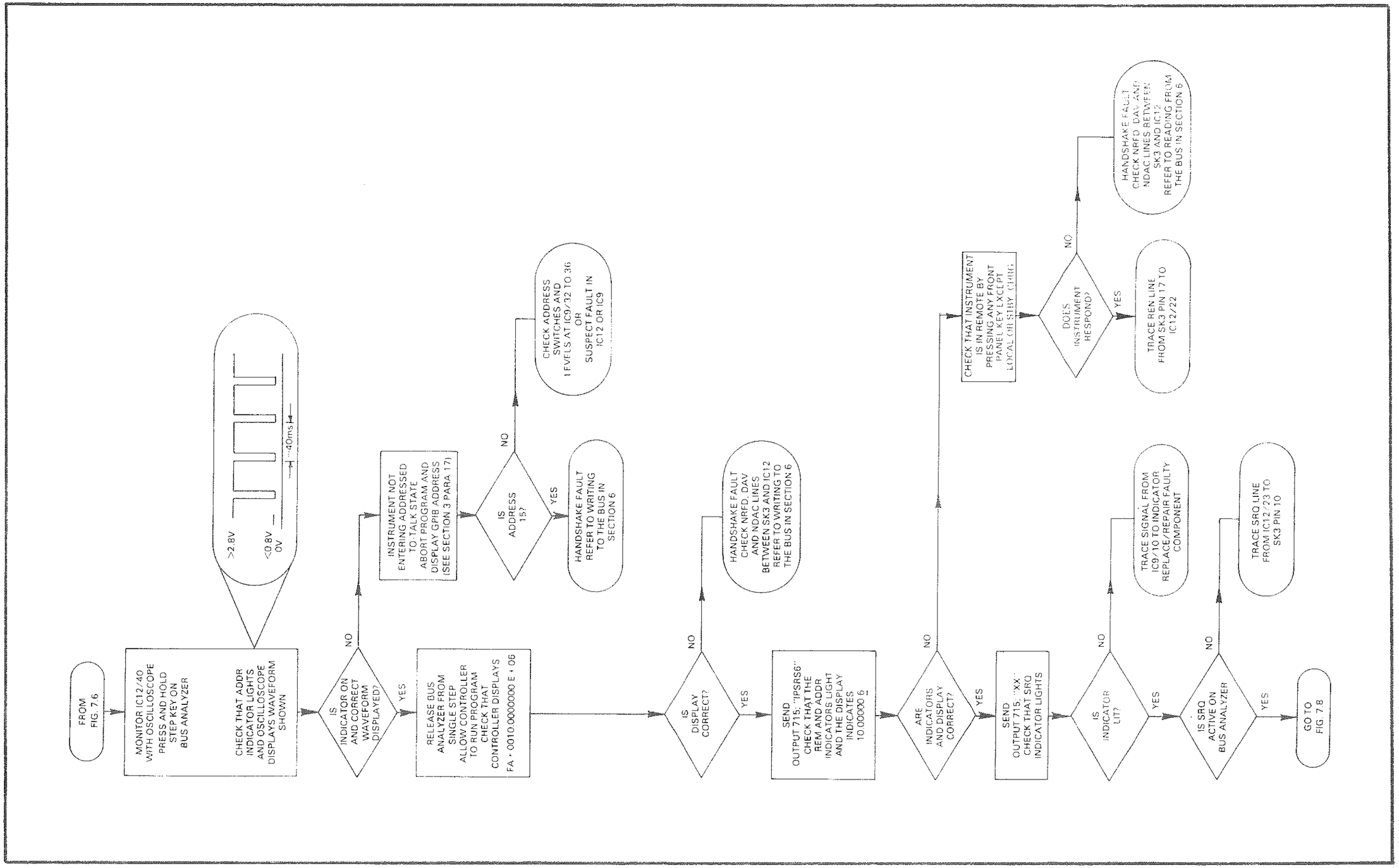


Fig 7.7 Fault Finding Flowchart GPIB Part 2

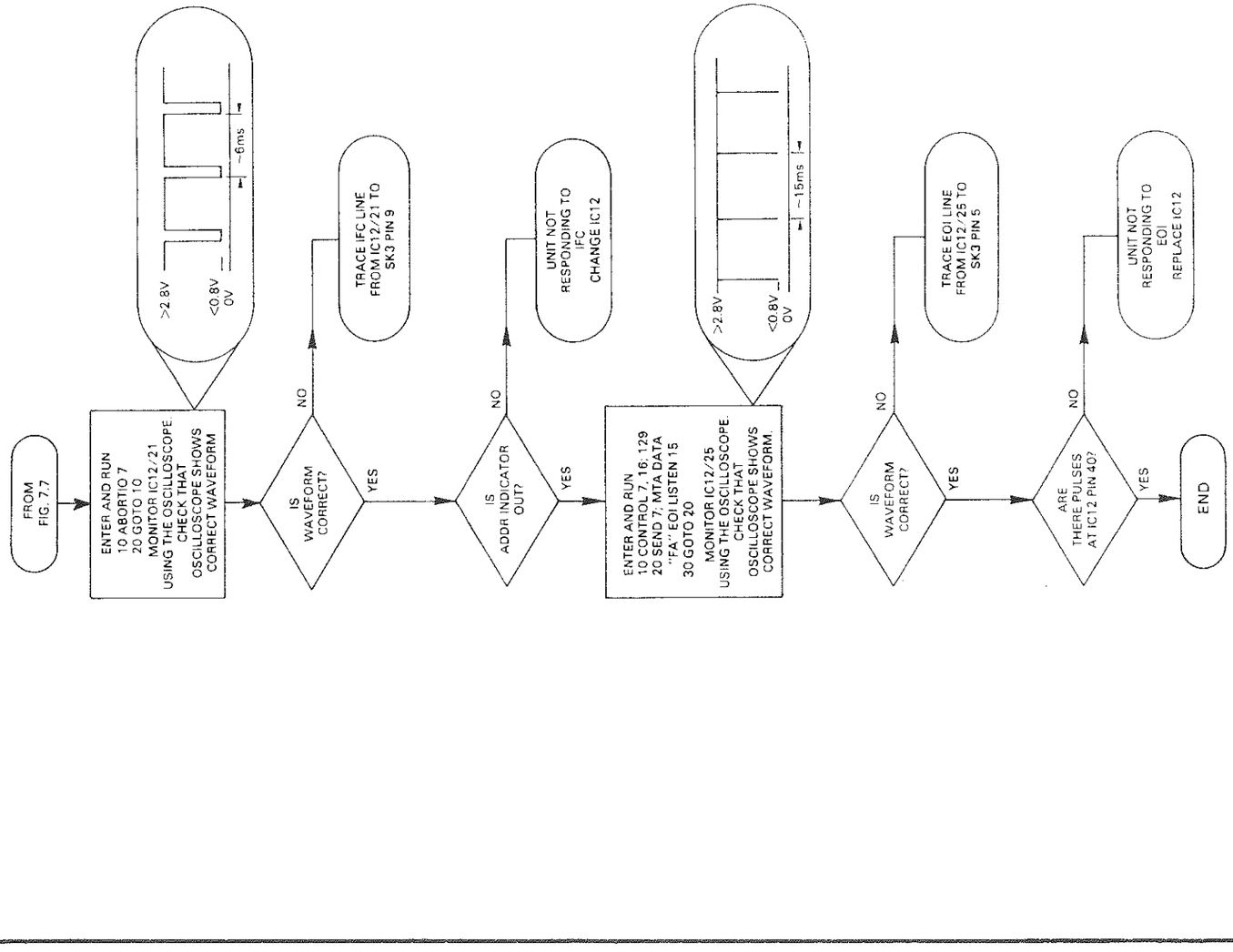


Fig 7.8 Fault Finding Flowchart GPIB Part 3

SETTING UP AFTER REPAIR

Introduction

28 After repair, the relevant setting-up procedures from those given in the following paragraphs should be implemented before carrying out the overall specification check. The procedures should also be used if the instrument fails a routine specification check. Unless otherwise stated the procedures are applicable to both the 1998 and 1999 instruments.

29 The ambient temperature must be maintained at 23 ^{o}C ± 2 ^{o}C throughout the procedures. The instrument should be powered from an AC supply, not a battery pack. A warm-up time of 10 minutes should be allowed before making any adjustment.

WARNING: LETHAL VOLTAGE
THESE PROCEDURES REQUIRE THE INSTRUMENT TO BE OPERATED WITH THE COVERS REMOVED. LETHAL VOLTAGE LEVELS ARE EXPOSED UNDER THESE CONDITIONS.

Channel A Input System

30 Test equipment required:

Item	Table 7.1 Item No.
Signal Generator	1
Digital Multimeter	3

31 Set R24 fully counter-clockwise and R19 to its mid-position. R24 and R19 are located inside the screened module on the motherboard 19-1160, as shown in Fig 7.9.

32 (1) Switch the 1998/1999 on. Select FREQ A and .

(2) Select 50 Ω impedance and disable the filter on the A channel.

(3) Set the SENSITIVITY control fully clockwise and select X1 attenuation.

(4) Press the RESOLUTION key five times, until 000 is displayed.

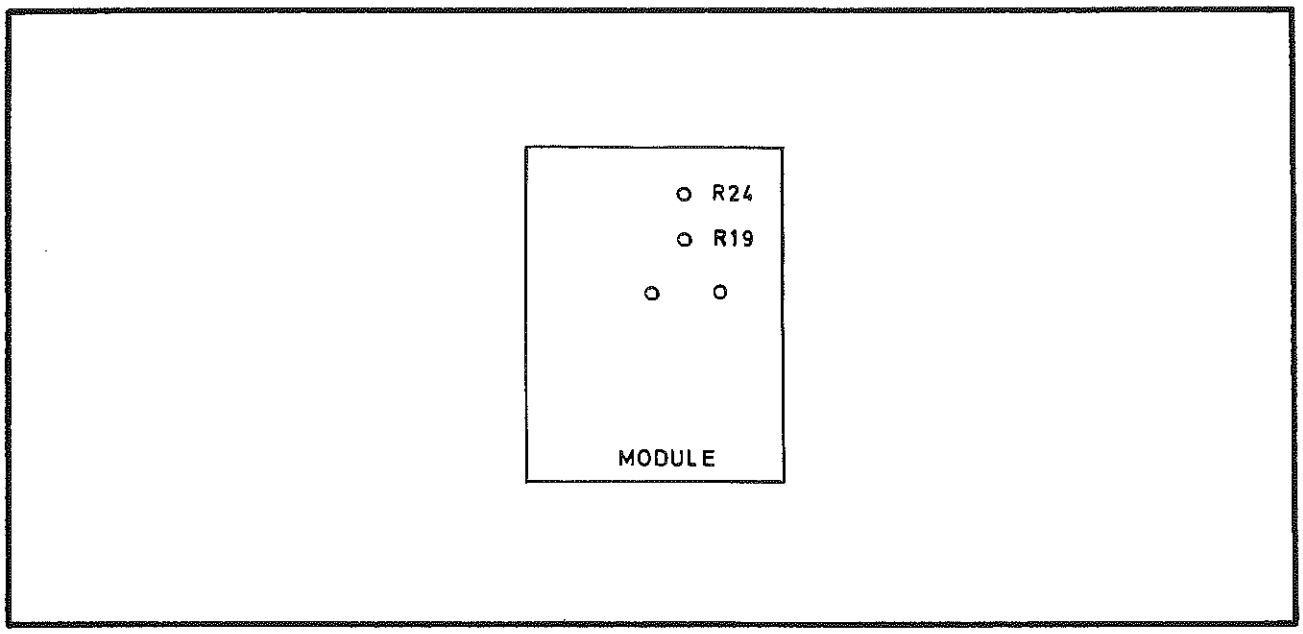


Fig 7.9 Location of R24 and R19

(5) Set the multimeter to measure voltages in the range +5 V to -5 V. With no signal at the A channel input, measure the voltage at TP3 on assembly 19-1237 with respect to 0 V. If necessary adjust R4 to give a voltage of 0 V ±50 mV. The locations of TP3 and R4 are shown in Fig 7.10.

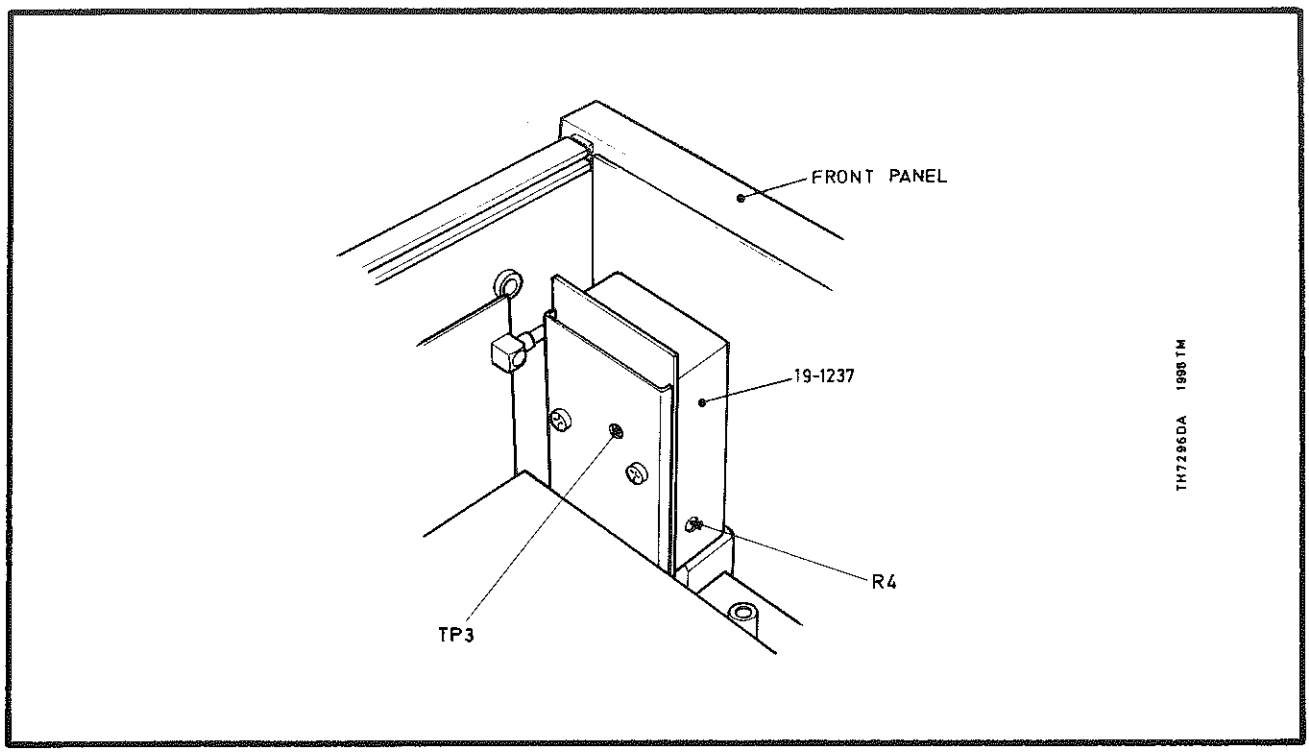


Fig 7.10 Location of TP3 and R4

(6) Connect the test equipment as shown in Fig 7.11.

(7) Set the signal generator output to 10 MHz at a level of 2.6 mV r.m.s.

(8) Verify that the EXT STD indicator is lit.

(9) Adjust R19 to obtain the most stable display indication of 10.00 MHz ±0.10 MHz with the GATE indicator flashing.

NOTE: Care is needed when adjusting R19. The display indication is random with R19 set to either side of the correct position.

(10) If a stable display of 10 MHz with the GATE indicator flashing cannot be obtained, increase the signal generator output level by 0.1 mV and repeat step (9). Steps (9) and (10) may be repeated, if necessary, up to a signal level of 4.0 mV.

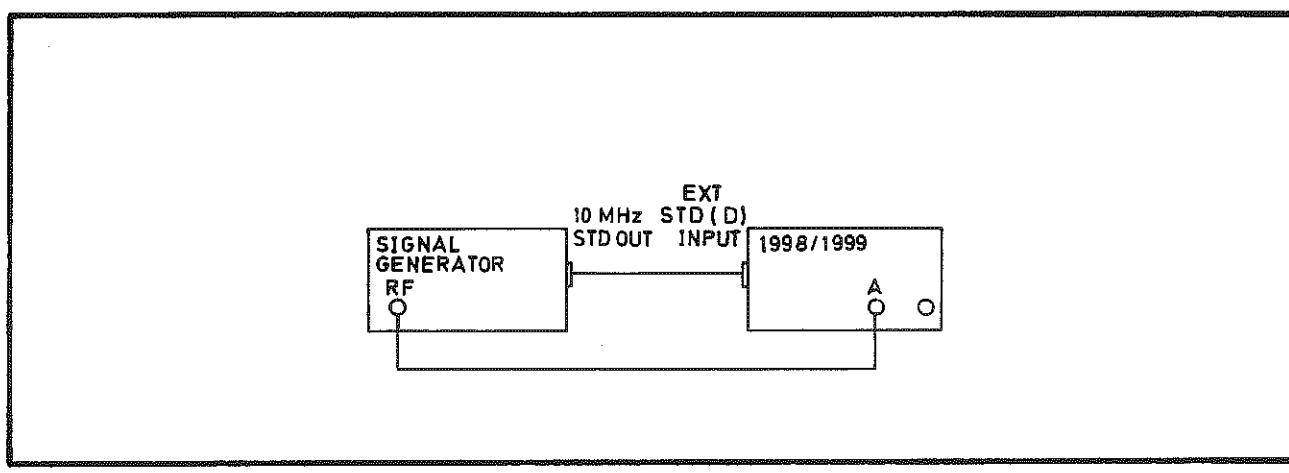


Fig 7.11 Connections for the Channel A Input System Adjustment

33 (1) Switch off the RF output of the signal generator.

(2) Press the RESOLUTION key five times, until 00000000 is displayed.

(3) Switch on the RF output of the signal generator.

(4) Set the signal generator output to 120 MHz at a level of 6.0 mV r.m.s.

(5) Adjust R24 slowly clockwise until the display just becomes unstable. Turn back until the display indicates 120.00000 MHz ± 0.00001 MHz and is just stable.

(6) Reduce the signal generator output to 3.7 mV r.m.s. Verify that the GATE indicator stops flashing. If it does not, repeat steps (4) to (6).

(7) Switch off the 1998/1999. Disconnect the test equipment.

Channel B Assembly 19-1142 (1998 only)

34 Test equipment required:

Item	Table 7.1 Item No.
Signal Generator	1
Coaxial Lead	7

35 Connect the test equipment as shown in Fig. 7.12.

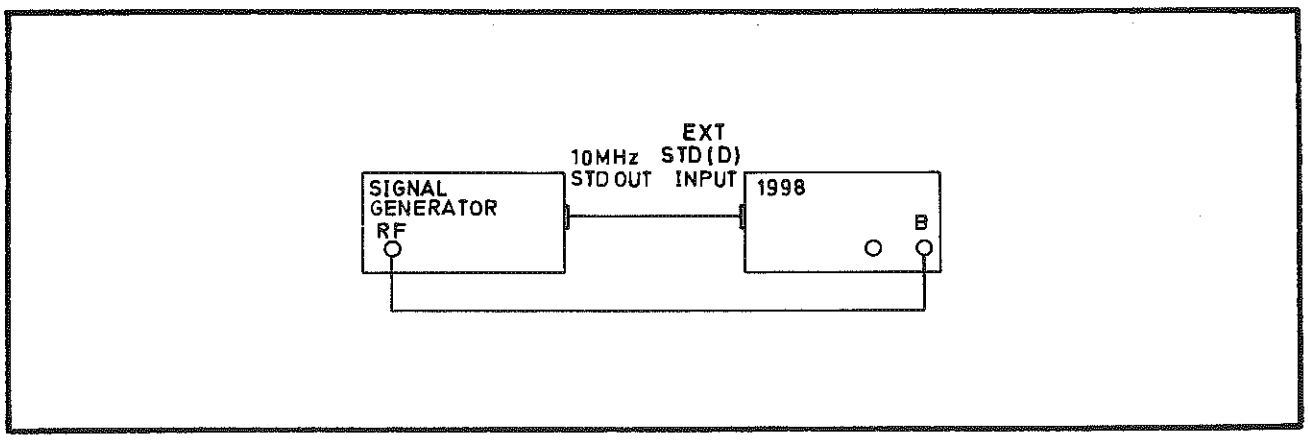


Fig 7.12 Connections for 1998 Channel B Input System Adjustment

36 (1) Set R27 on assembly 19-1142 fully clockwise.

(2) Switch the 1998 on. Select FREQ B. Verify that the EXT STD indicator is lit.

(3) Set the signal generator output to 1 GHz at a level of 5.0 mV r.m.s.

(4) Adjust R27 until the gate indicator just starts flashing and the 1998 display indicates 1000.00000 MHz ± 0.00001 MHz.

(5) Switch the output of the signal generator off. Reduce the output level to 4.5 mV r.m.s.

(6) Switch the output of the signal generator on. Verify that the 1998 is not counting. If it is, repeat steps (3) to (6).

(7) Switch off the 1998. Disconnect the test equipment.

Channel B Assembly 19-1300 (1999 only)

37 Test equipment required:

Item	Table 7.1 Item No.
Signal Generator	1
Digital Multimeter	3
True RMS Millivoltmeter	14
Power Supply	15
T Splitter	16
Test Lead	17
Test Lead	18

38 The AGC Threshold must be checked before proceeding with either the Overload Threshold or the Low Level Inhibit Threshold checks. Further, if the AGC Threshold is adjusted both the Overload Threshold and the Low Level Inhibit Threshold must be reset.

AGC Threshold

39 Connect the test equipment as shown in Fig 7.13. The screening assembly must be fitted to assembly 19-1300.

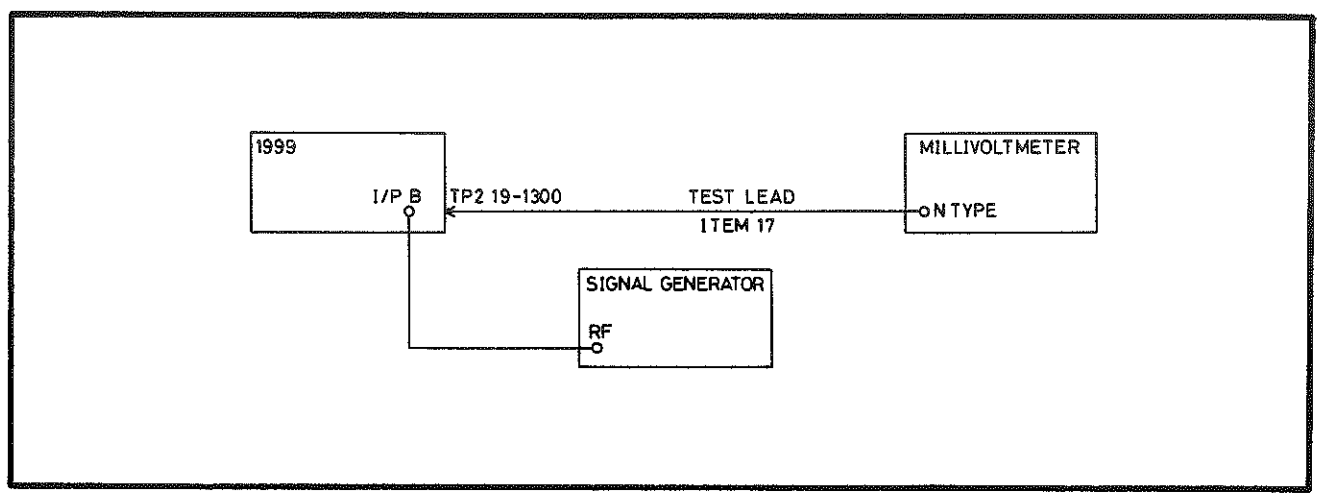


Fig 7.13 Connections for AGC Threshold Adjustment

40 Switch on the 1999 and the test equipment. Set the signal generator output to 80 MHz with modulation off.

41 (1) Rotate R39 on assembly 19-1300 (see Fig 7.14) fully anticlockwise.

(2) Adjust the signal generator output until the millivoltmeter indicates 0 dBm ± 0.2 dBm.

(3) Rotate R39 on assembly 19-1300 clockwise until the millivoltmeter indicates -3 dBm ± 0.5 dBm.

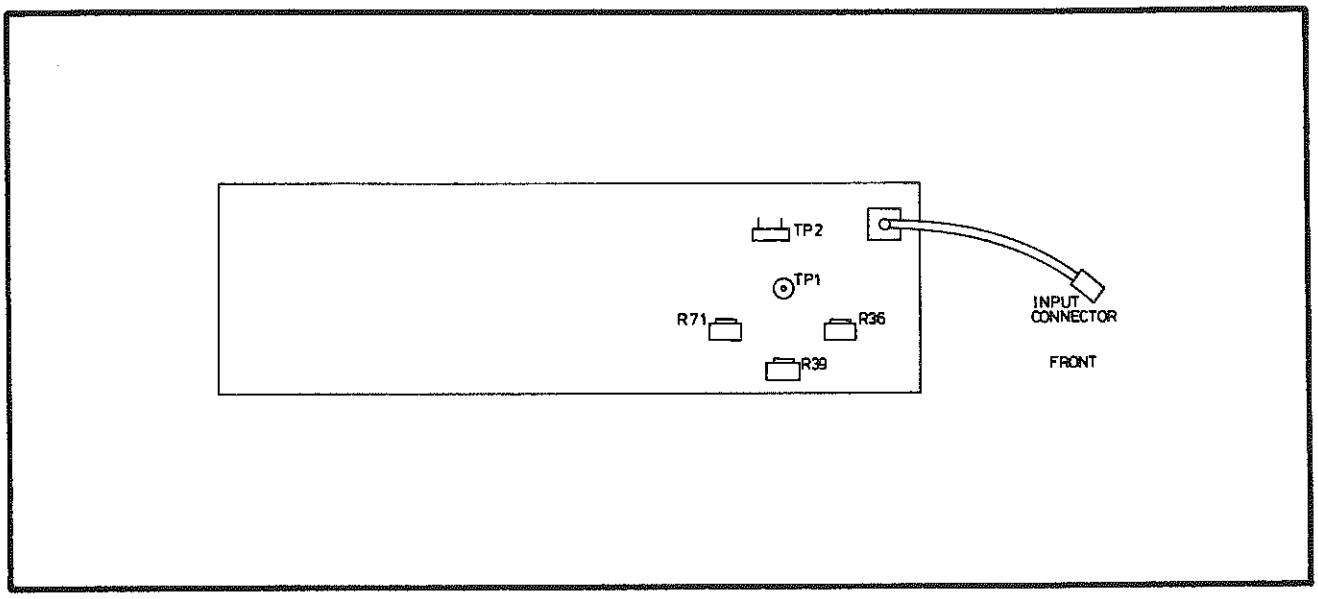


Fig 7.14 Assembly 19-1300: Location of Potentiometers

42 Switch off the 1999 and test equipment. Disconnect the test equipment.

Overload Threshold

43 Connect the test equipment as shown in Fig 7.15.

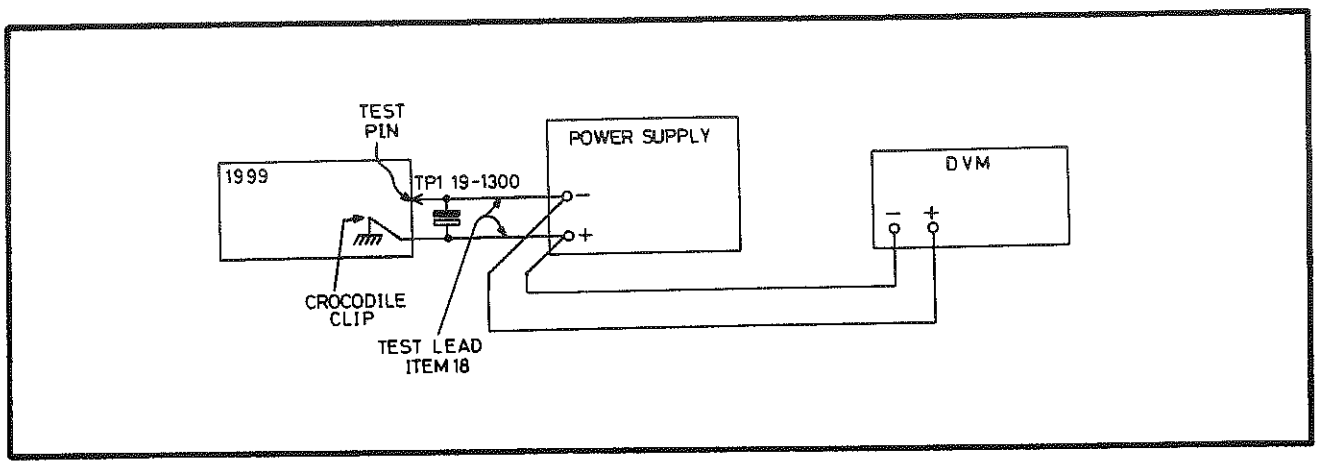


Fig 7.15 Connections for 19-1300 Overload Threshold Adjustment

44 (1) Rotate R36 on assembly 19-1300 (see Fig 7.14) fully anticlockwise.

(2) Switch on the 1999 and the power supply.

45 Adjust the power supply until the multimeter indicates 8.65 V ± 50 mV.

46 (1) Rotate R36 on assembly 19-1300 until the OVERLOAD indicator on the front panel just lights.

(2) Disconnect the test connection to TP1 on assembly 19-1300.

(3) Adjust the power supply output voltage to 8.35 V ± 50 mV.

(4) Reconnect the test connection to TP1.

(5) Verify that the OVERLOAD indicator is extinguished.

(6) If the indicator is lit, repeat Paragraphs 45 and 46

47 Switch off the 1999 and test equipment. Disconnect the test equipment.

Low-level Inhibit Threshold

48 Connect the test equipment as shown in Fig 7.16.

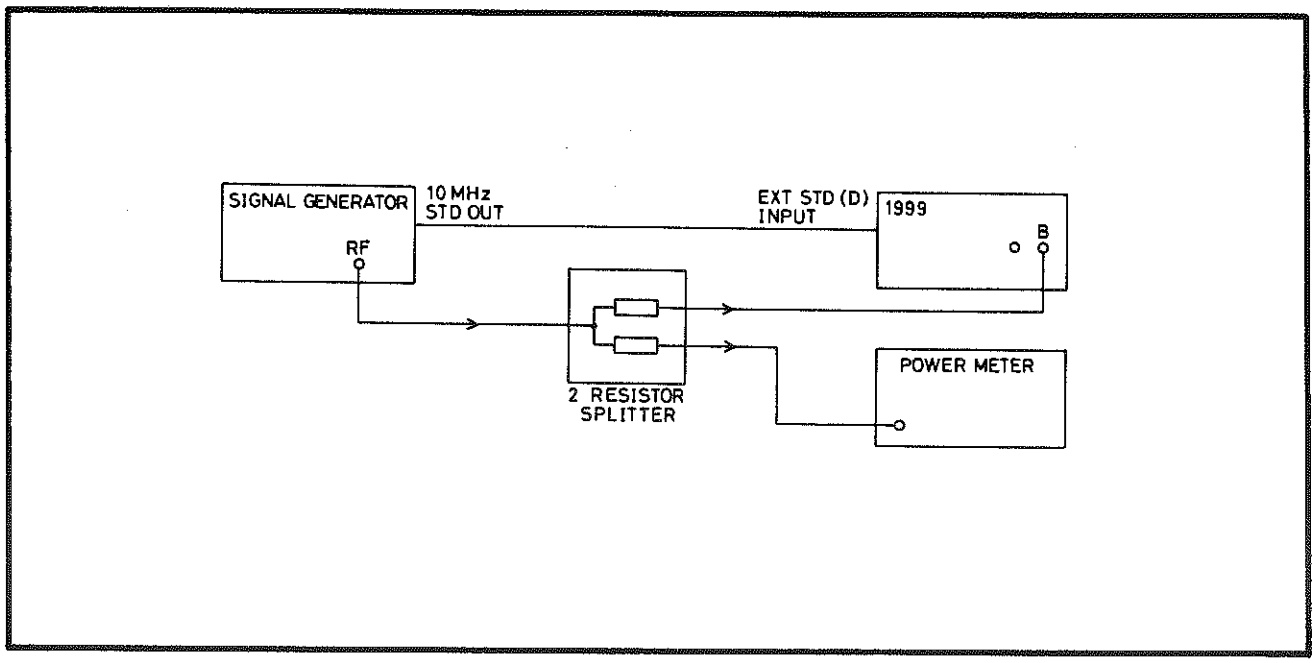


Fig 7.16 Connections for Low-Level Inhibit Threshold Adjustment

49 (1) Rotate R71 on assembly 19-1300 (see Fig 7.14) fully anticlockwise.

(2) Switch on the 1999 and select FREQ B. Verify that the EXT STD indicator is lit.

(3) Set the signal generator output to 80 MHz. Adjust the output level until the power meter indicates -30.2 dBm ± 0.2 dm.

(4) Adjust R71 clockwise until the 1999 front panel GATE indicator just commences to flash. Verify that the display indicates 80.000000 MHz ± 0.000001 MHz.

(5) Reduce the signal generator output to -30.8 dBm ± 0.2 dBm.

(6) Verify that the 1999 is not counting.

(7) If the 1999 is counting repeat steps (3) to (6).

(8) Switch off the 1999 and test equipment. Disconnect the test equipment.

Frequency Doubler 19-1238 (Options 04A and 04B only)

50 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope with X10 Probe	2
Trimming Tool	13

51 (1) Switch on the 1998/1999. Allow a warm-up period of 10 minutes for option 04A and 30 minutes for option 04B.

(2) Monitor the signal at pin 3 using the oscilloscope and X10 probe. Verify that the frequency is 10 MHz.

(3) If necessary, adjust T1 and T2 to obtain a signal level not less than 0.5 V peak-to-peak.

(4) Monitor the DC voltage at TP1 using the oscilloscope and X10 probe. Adjust T1 and T2 to obtain the smallest possible voltage. Verify that the voltage achieved is in the range from 400 mV to 800 mV.

(5) Transfer the probe to pin 3. Verify that the signal frequency is 10 MHz and that the level is in the range from 0.8 V to 1.2 V.

(6) Switch off the 1998/1999. Disconnect the test equipment

External Reference Multiplier 19-1164 (Option 10)

52 Test equipment required

Item	Table 7.1 Item No.
Oscilloscope with X10 Probe	2
Frequency Standard	4
Coaxial Lead	7
Trimming Tool	13

53 (1) Switch the 1998/1999 on.

(2) Connect the frequency standard to the EXT. STD. (D) INPUT socket. Verify that the EXT STD indicator lights.

(3) Monitor the DC voltage at TP1 using the oscilloscope and X10 probe.

(4) If necessary, adjust C2 to obtain a voltage of +2.5V ±0.2V.

(5) Switch off the 1998/1999. Disconnect the test equipment.

INTERNAL FREQUENCY STANDARD, ROUTINE CALIBRATION

54 Test equipment required:

Item	Table 7.1 Item No.
Frequency Standard	4
Coaxial lead	7

NOTE: If an Option 04A (9444) or Option 04B (9423) frequency standard is fitted, allow the instrument to warm up for 24 hours (switched to standby, if required) before making any adjustment.

55 (1) Switch on the 1998/1999. Select FREQ A and verify that 00000000 is displayed. If the Option 04B (9423) frequency standard is fitted, press the RESOLUTION ↓ key until 000000000 is displayed.

(2) Connect the 10 MHz STD OUTPUT socket to the A channel input, using the coaxial lead.

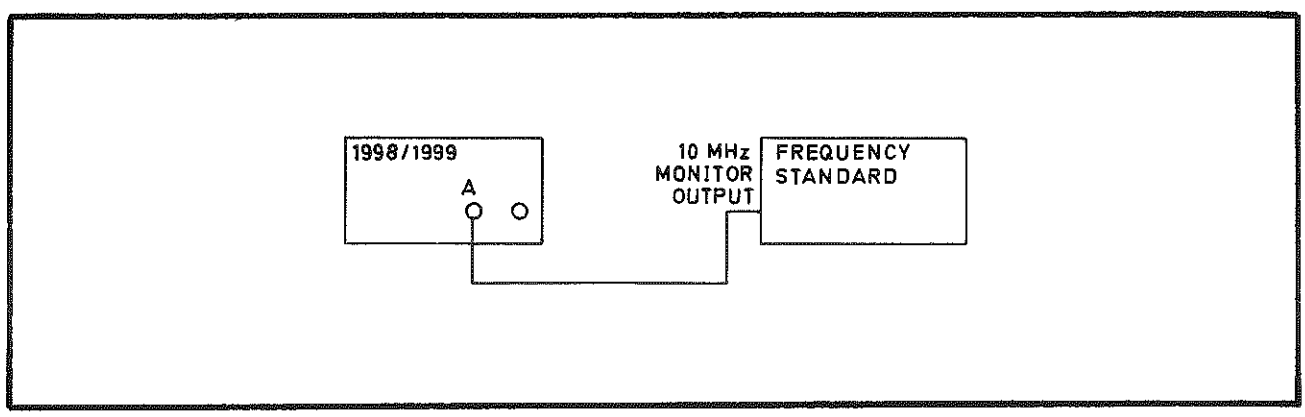


Fig 7.17 Connections for Internal Frequency Standard Adjustment

(3) Press NULL .

(4) Disconnect the signal from the A channel input.

(5) Connect the frequency standard as shown in Fig 7.17.

(6) Adjust the internal frequency standard, via the aperture in the rear panel, to be as near to 10 MHz as possible. The display limits are shown in Table 7.3.

(7) Switch off the 1998/1999. Switch off and disconnect the test equipment.

TABLE 7.3

Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Standard Oscillator	±5.0 Hz	5 parts in 10^7
Option 04T	±1.0 Hz	1 part in 10^7
Option 04A (9444)	±0.1 Hz	1 part in 10^8
Option 04B (9423)	±0.01 Hz	1 part in 10^9

BATTERY PACK 11-1625 (OPTION 07)

56 Test equipment required:

Item	Table 7.1 Item No
Digital Multimeter	3
Multimeter, 2 off	23
Power Supply	15
Test Lead	24

NOTES:

(1) The battery pack should be installed in the parent 1998/1999.

(2) The battery tray should be in position, but disconnected at the flying lead (SK12/PL12).

(3) The numbers on mating pins of PL21 on the Motherboard Assembly 19-1160 and SK21 on the Battery Pack Assembly 11-1625 do not correspond,see Fig.23 in Section 8. Take care to connect test equipment to the points specified. Connection must be made to PL21 from the underside of the motherboard.

57 Connect the test equipment as shown in Fig 7.18. DO NOT CONNECT THE 1998/1999 TO AN AC SUPPLY.

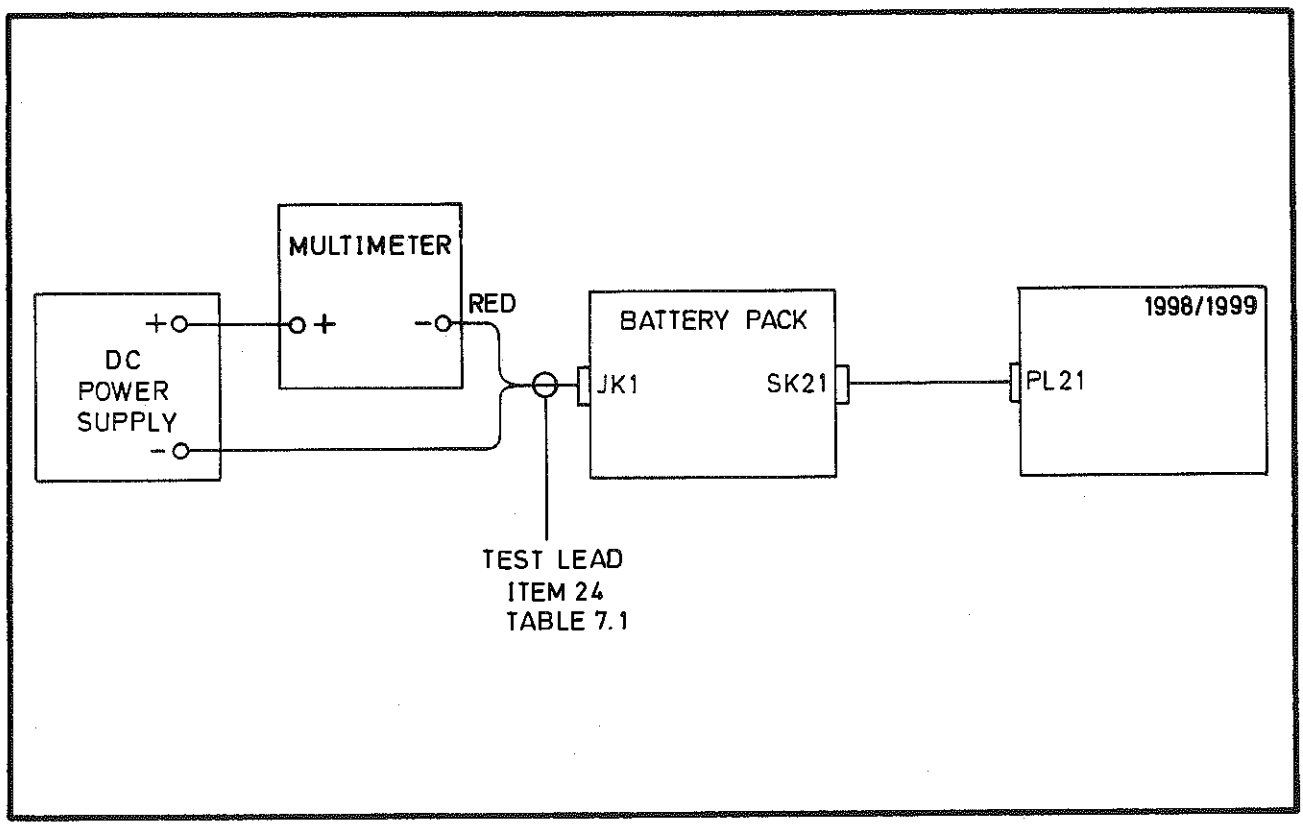


Fig 7.18 Connections for Battery Pack Test

58 (1) Set R10, R28 and R36 on the battery pack fully clockwise.

(2) Set the INTERNAL/EXTERNAL switch to EXTERNAL.

(3) Set the NORMAL/BATTERY SAVE switch to NORMAL.

59 (1) Set the multimeter to measure direct current greater than 2 A.

(2) Set the power supply output to 15 V.

(3) Switch on the 1998/1999. Verify that the normal start-up sequence occurs.

60 (1) Set the digital multimeter to measure over the range from 4 V to 20 V DC.

(2) Connect the digital multimeter between PL21 pin 4 (positive) and PL21 pin 10 (0 V).

(3) If necessary, adjust R28 on the battery pack to obtain an indication of between 5.38 V and 5.40 V.

61 Use the digital multimeter to measure the voltage between PL21 pin 10 (0 V) and each of the points shown in Table 7.4. Verify that the voltages measured are as shown in column A.

TABLE 7.4

Battery Pack Voltage Levels

Test Point	Voltage Relative to PL21 Pin 10	
	A	B
PL21 pin 4	+5.38 V to +5.40 V	+5.36 V to +5.40 V
PL21 pin 5	-5.50 V to -5.95 V	-5.45 V to -6.00 V
PL21 pin 15	+14.50 V to +15.70 V	+14.40 V to +15.80 V
PL21 pin 14	-14.55 V to -15.75 V	-14.45 V to -15.85 V

62 Transfer the digital multimeter to measure the voltage between PL21 pin 19 (positive) and PL21 pin 10 (0 V). Adjust the power supply output to obtain an indication of 10.0 V to 10.2 V.

63 Use the digital multimeter to measure the voltage between PL21 pin 10 (0 V) and each of the points shown in Table 7.4. Verify that the voltages measured are as shown in column B.

64 (1) Turn R10 slowly counter-clockwise until the 1998/1999 shuts down completely (all display LEDs go out).

(2) Verify that the current drawn from the power supply immediately after the 1998/1999 shuts down, as indicated on the multimeter, is less than 50 µA (reduce the multimeter range as required).

(3) Verify that the current continues to fall towards zero.

(4) Set the multimeter to measure direct current greater than 2 A.

65 (1) Connect the digital multimeter between PL12 pin 1 (positive) and PL12 pin 3 (negative).

(2) Restore the power supply output to 15 V.

(3) Switch the 1998/1999 off and on. Wait until the start-up sequence is completed.

(4) Verify that the digital multimeter indicates not more than 0.1 V.

(5) Switch the 1998/1999 to standby.

(6) If necessary adjust R36 on the battery pack until the digital multimeter indicates between 7.62 V and 7.64 V.

(7) Switch the 1998/1999 off. Disconnect the digital multimeter.

66 (1) Set the second multimeter to measure direct current greater than 1.5 A.

(2) Connect the multimeter between PL12 pin 1 (positive) and PL12 pin 3 (negative).

(3) Disconnect the power supply and the first multimeter. Connect the 1998/1999 to an AC supply.

(4) Switch the 1998/1999 on. Wait until the start-up sequence is completed.

(5) Switch the 1998/1999 to standby. Verify that the current between PL12 pin 1 and PL12 pin 3 is between 0.9 A and 1.1 A.

(6) Switch the 1998/1999 off.

67 (1) Disconnect the multimeter from PL12.

(2) Connect the battery at PL12/SK12.

(3) Select INTERNAL. If necessary, switch the 1998/1999 on and select STANDBY to charge the battery. Switch the 1998/1999 off when charged.

(4) Disconnect the 1998/1999 from the AC supply.

(5) Switch the 1998/1999 on. Verify that the instrument can be switched in and out of standby.

(6) Switch the 1998/1999 off. Lock R10, R28 and R36 with a small quantity of silicone rubber.

OVERALL SPECIFICATION CHECK

Introduction

68 Satisfactory completion of the following performance verification procedures (PVPs) will confirm that the instrument is functional and meets its specification. Before commencing the specification check ensure that the instrument passes the test given in Section 3 Paragraphs 9 and 10. The PVPs should be carried out in the order given.

69 The following conditions must be maintained throughout the specification check:

(1) The instrument must be operated from an AC supply.

(2) The line voltage must be within the range indicated by the line voltage selector.

(3) The instrument covers must be fitted.

(4) The ambient temperature must be 23°C ± 2°C.

(5) The power supply to the frequency standard must be uninterrupted.

70 The instrument should be allowed to warm up for one hour (switched to standby, if required) before commencing the specification check. If Options 04A or 04B is fitted, allow the instrument to warm up for 24 hours.

Channel A Sensitivity PVP

71 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8

Audio Frequency Sensitivity PVP

72 (1) Switch on the 1998/1999. Select 50 Ω on the A channel. Turn the SENSITIVITY control fully clockwise.

(2) Connect the test equipment as shown in Fig 7.19. Check that the EXT STD indicator lights.

(3) Set the signal generator output to the frequencies shown in Table 7.5 in turn. Set the 1998/1999 resolution to the corresponding value.

(4) At each frequency, determine the minimum input level to the 1998/1999 which gives stable counting. Verify that this is not more than the level shown in the table.

(5) Disconnect the test equipment.

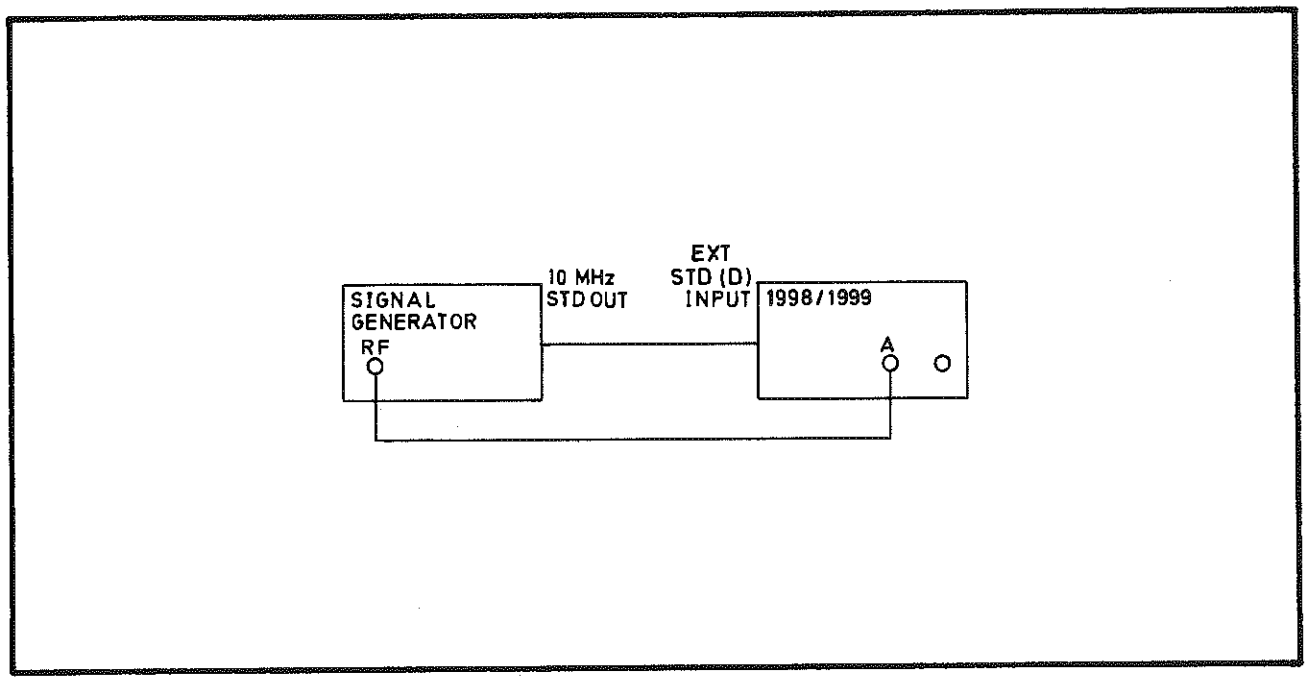


Fig 7.19 Connections for the Channel A Sensitivity PVP

TABLE 7.5

Channel A Sensitivity

Frequency	1998/1999 Resolution	Signal Level
160 MHz	8 digits	42 mV
120 MHz	8 digits	8.5 mV
10 MHz	7 digits	8.5 mV
100 kHz	5 digits	8.5 mV

RF Frequency Sensitivity PVP

73 (1) Connect the test equipment as shown in Fig 7.20.

(2) Set the audio oscillator output to the frequencies shown in Table 7.6 in turn. Set the 1998/1999 resolution to the corresponding value. Enable the 50 kHz filter.

(3) At each frequency, determine the minimum input level to the 1998/1999 which gives stable counting. Verify that this is not more than the level shown in the table.

(4) Disable the 50 kHz filter

(5) Disconnect the test equipment.

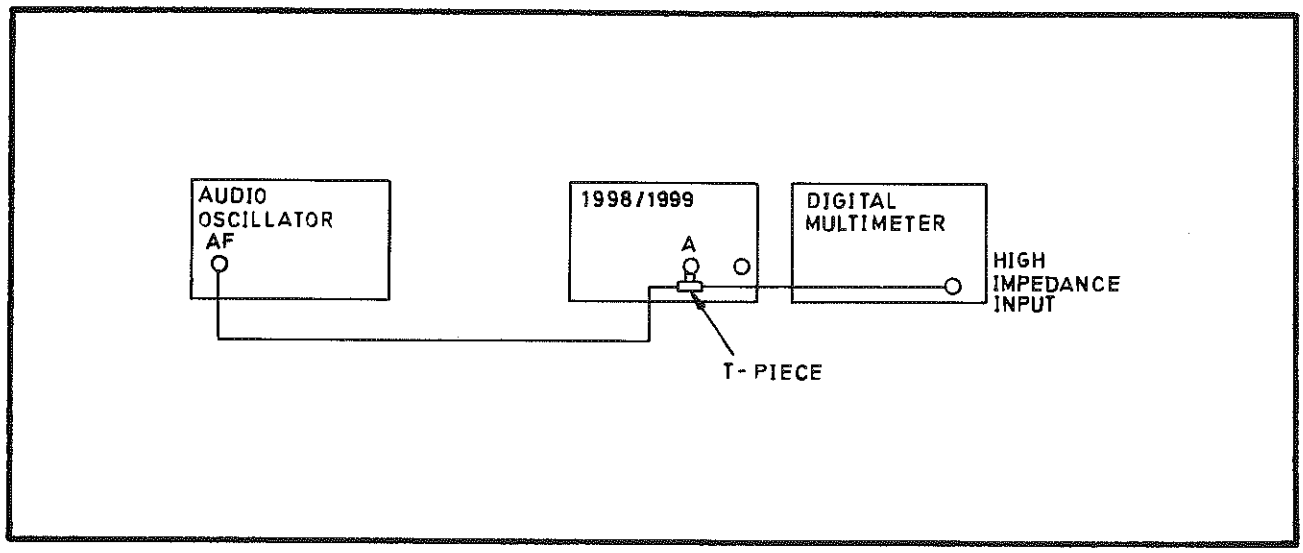


Fig 7.20 Connections for the Channel A Sensitivity PVP

TABLE 7.6

Channel A Sensitivity

Frequency	1998/1999 Resolution	Signal Level
5 kHz	3 digits	8.5 mV
10 Hz	3 digits	17 mV

Channel A Pulse Offset PVP

74 Test equipment required:

Item	Table 7.1 Item No.
Pulse Generator	6
Attenuator	10

75 (1) Connect the test equipment as shown in Fig 7.21

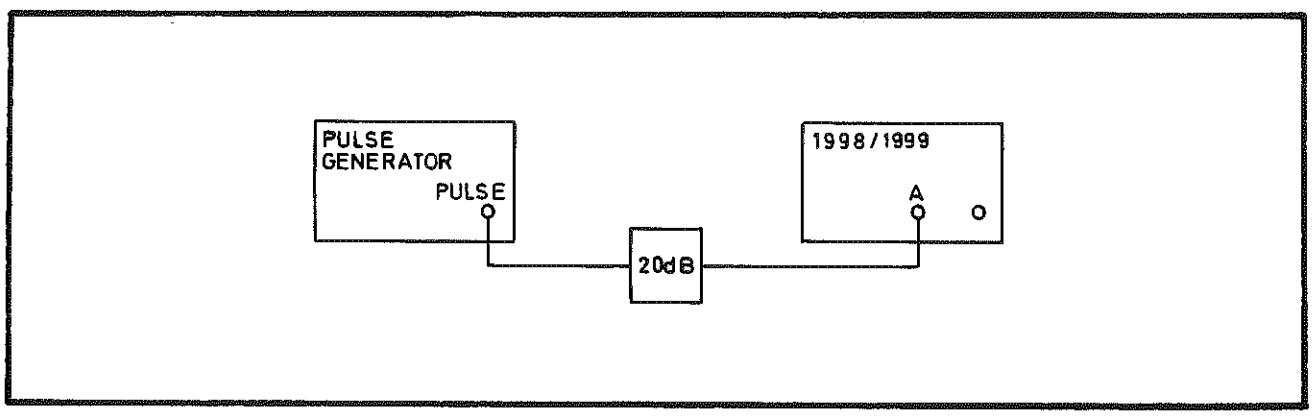


Fig 7.21 Connections for the Channel A Pulse Offset PVP

(2) Set the pulse generator to give positive-going pulses with an amplitude of 250 mV peak-to-peak. Set the pulse repetition frequency to 100 kHz and the duty cycle to 10%.

(3) Select ⎍, ∿ and ⎎ pulse offset in turn. Verify that the instrument functions as shown in Table 7.7.

TABLE 7.7

Pulse Offset PVP

Pulse Polarity	Pulse Offset		
	⎍	∿	⎎
Positive-going	100 kHz (see note)	Not gating	Not gating
Negative-going	Not gating	Not gating	100 kHz (see note)

Note: The display must be stable. The exact frequency displayed is not critical, but it must not be a multiple of the input frequency.

(4) Set the pulse generator to give negative-going pulses and repeat step (3).

(5) Select ∿. Disconnect the test equipment.

Channel A Attenuator, SENSITIVITY Control and Filter PVP.

76 Test equipment required:

Item	Table 7.1 Item No.
Signal Generator	1

77 Connect the test equipment as shown in Fig 7.22. Verify that the EXT STD indicator lights.

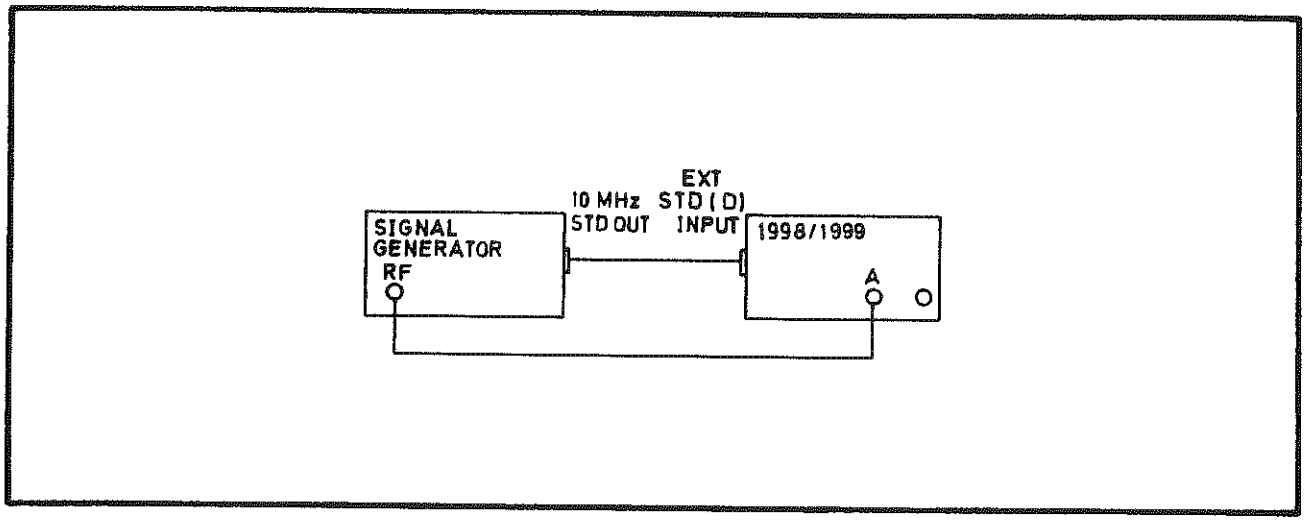


Fig 7.22 Connections for Channel A Attenuator PVP

78 (1) Set the signal generator output to 1 MHz ±1 Hz. Set the 1998/1999 to 8-digit resolution.

(2) Measure the A channel sensitivity, to a resolution of 0.1 mV, by determining the minimum input to the 1998/1999 which gives stable counting. Record this level.

(3) Enable the X20 attenuator and measure the A channel sensitivity to a resolution of 1 mV.

(4) Verify that the ratio of the levels obtained in (3) and (2) is in the range from 15 to 25.

(5) Disable the X20 attenuator and turn the SENSITIVITY control fully counter-clockwise.

(6) Measure the A channel sensitivity to a resolution of 1 mV.

(7) Verify that the ratio of the levels obtained in (6) and (2) is in the range from 19 to 53.

(8) Turn the SENSITIVITY control fully clockwise.

(9) Set the signal generator output to 50 kHz at a level of 50 mV r.m.s. Verify that the 1998 indicates 50 kHz ±1 Hz.

(10) Enable the filter. Verify that the 1998/1999 still indicates 50 kHz ±1 Hz.

(11) Set the signal generator frequency to 10 MHz. Verify that the 1998/1999 stops gating.

(12) Disable the filter. Disconnect the test equipment.

Channel A 50 Ω Load PVP

79 Test equipment required:

Item	Table 7.1 Item No.
Digital Multimeter	3

80 (1) Select 1 MΩ input impedance.

(2) Connect the multimeter to measure the input resistance of the A channel. Verify that the resistance is greater than 1.5 MΩ.

(3) Select 50Ω input resistance. Verify that the resistance is in the range 46 Ω to 54 Ω.

(4) Disconnect the test equipment.

1998 Channel B Sensitivity PVP

81 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
Coaxial Lead	7

82 (1) Connect the test equipment as shown in Fig 7.23. Verify that the EXT STD indicator lights.

(2) Select FREQ B.

(3) Set the signal generator output to the frequencies shown in Table 7.8 in turn. Set the 1998 gate time to the corresponding value.

(4) At each frequency, determine the minimum input level to the 1998 which gives stable counting. Verify that this is not more than the level shown in the table.

(5) Disconnect the test equipment.

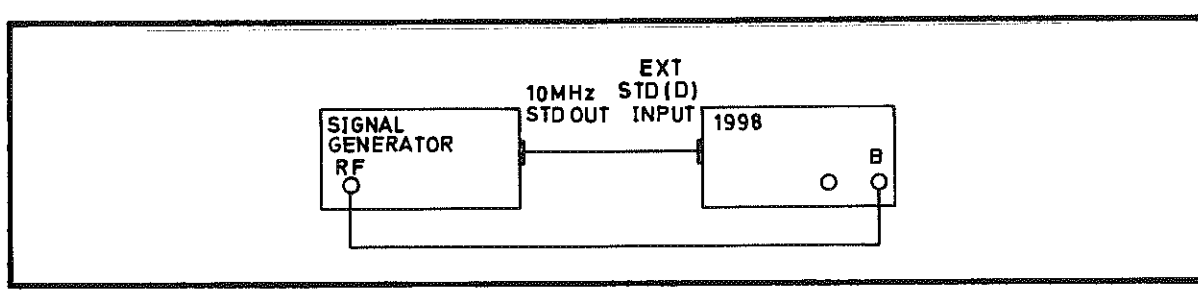


Fig 7.23 Connections for the 1998 Channel B Sensitivity PVP

TABLE 7.8

1998 Channel B Sensitivity

Frequency	1998 Gate Time	Signal Level
40 MHz	100 ms	8.5 mV
100 MHz	100 ms	8.5 mV
500 MHz	100 ms	8.5 mV
1000 MHz	1 s	8.5 mV
1300 MHz	1 s	70 mV

1999 Channel B Sensitivity PVP

83 Test equipment required:

Item	Table 7.1 Item No
Power Meter	19
Signal Generator	20
Power Splitter	16
Attenuator	21
Coaxial Adaptors (N to BNC)	22
Connecting Leads	7
Coaxial Adaptors (N to N)	25

NOTE:
If test equipment other than that specified in Table 7.1 is used, other accessories may be required.

84 (1) Connect the test equipment as shown in Fig 7.24. Verify that the EXT STD indicator lights.

(2) Select FREQ B.

(3) Set the signal generator output to the frequencies shown in Table 7.9 in turn. Set the 1999 gate time to the corresponding value.

(4) At each frequency, determine the minimum input level to the 1999, as indicated on the power meter, which gives stable counting. Verify that this is not more than the level shown in the table.

(5) Disconnect the test equipment.

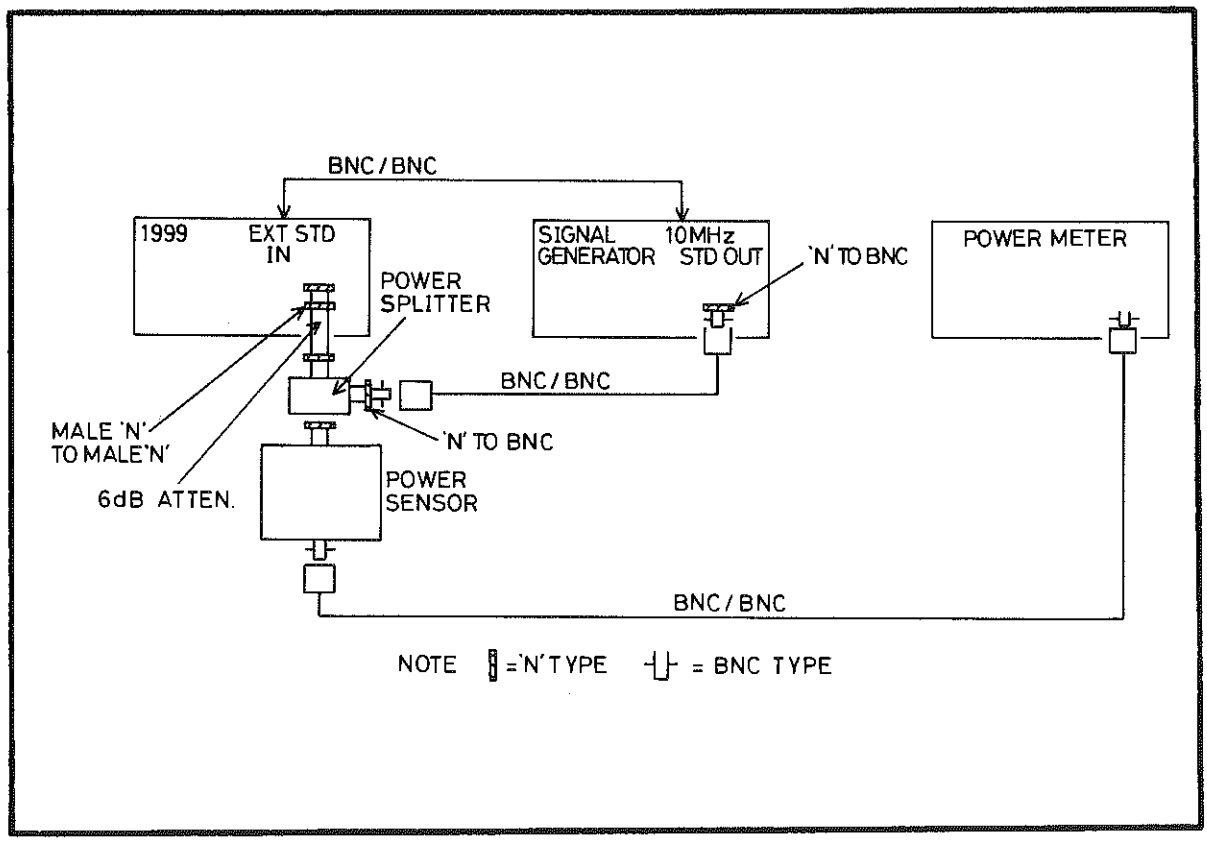


Fig 7.24 Connections for the 1999 Channel B Sensitivity PVP

TABLE 7.9

1999 Channel B Sensitivity

Frequency	1999 Gate Time	Signal Level
80 MHz	100 ms	8.5 mV
500 MHz	100 ms	8.5 mV
1000 MHz	1 s	8.5 mV
1500 MHz	1 s	8.5 mV
2000 MHz	1 s	8.5 mV
2600 MHz	1 s	8.5 mV

External Standard (D) Input Sensitivity PVP

85 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	1
T-piece	8

86 (1) Connect the test equipment as shown in Fig 7.25.

(2) Select RATIO A/D, 50 Ω input impedance and 100 ms gate time.

(3) Set the signal generator output to 10 MHz at a level of 10 mV.

(4) Slowly increase the signal level until the 1998/1999 indicates 1.000000 ± 0.000001.

(5) Verify that the signal level is not more than 80 mV r.m.s.

(6) Set the signal generator output to 10 kHz at a level of 10 mV.

(7) Repeat steps (4) and (5) with the display reading 1.000 ± 0.001.

(8) Disconnect the test equipment.

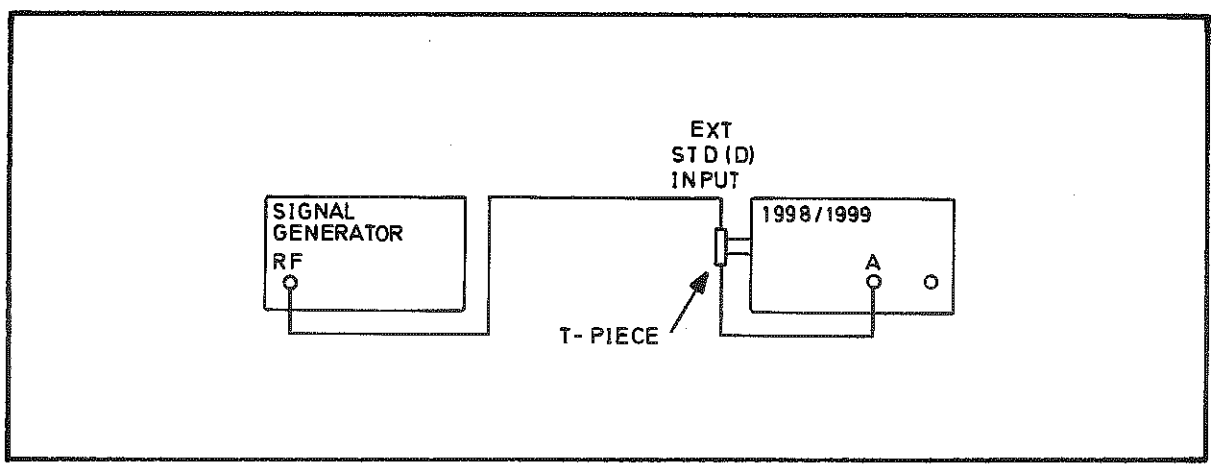


Fig 7.25 Connections for External Standard (D) Input PVP

10 MHz Standard Output Level PVP

87 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	2
T-piece	8
Load	9

88 (1) Connect the test equipment as shown in Fig 7.26.

(2) Verify that the peak-to-peak amplitude of the displayed waveform is 1.0 V ±0.4 V. Verify that the mark/space ratio is between 30:70 and 70:30.

(3) Disconnect the test equipment.

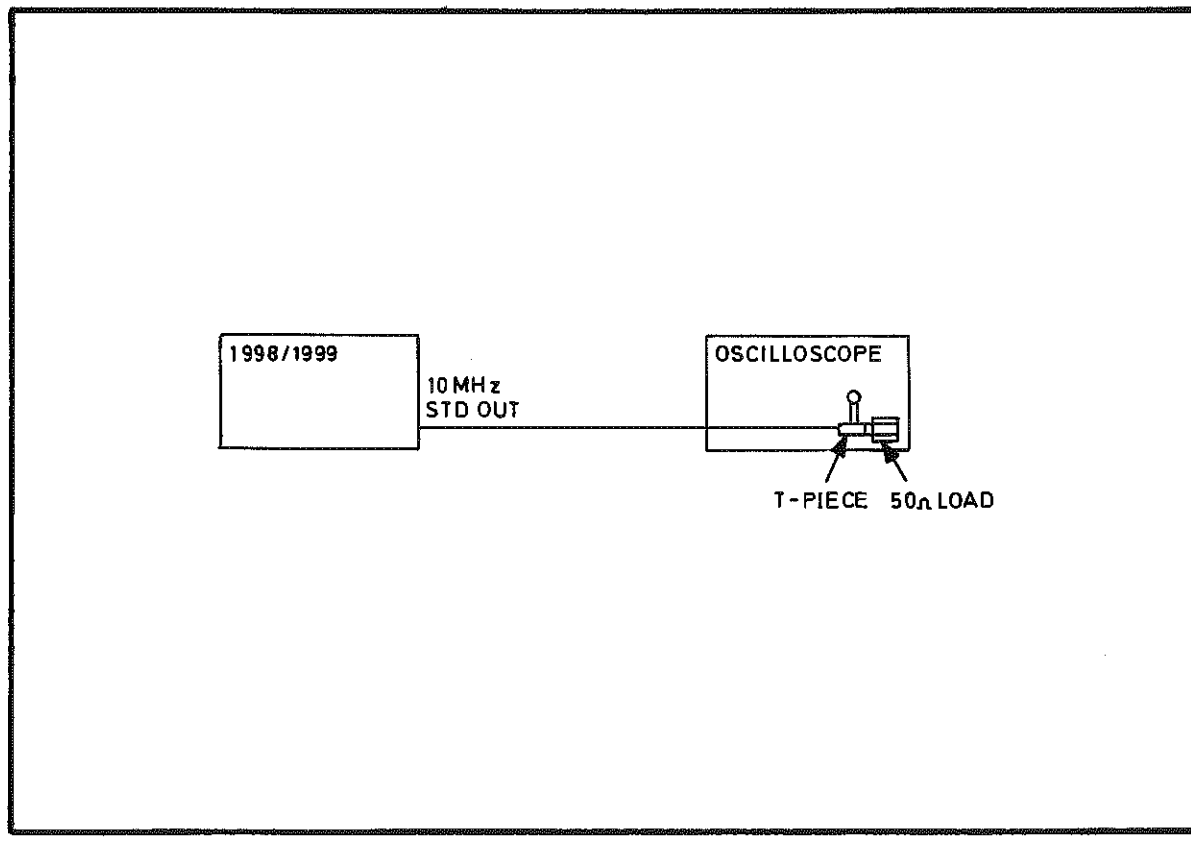


Fig 7.26 Connections for 10 MHz Standard Output Level PVP

External Arming PVP

89 Test equipment required

Item	Table 7.1 Item No
Pulse Generator	6
T-piece	8
Load	9

90 (1) Select FREQ A.

(2) Connect the test equipment as shown in Fig 7.27.

(3) Prepare the pulse generator to give a single, 300 µs, positive-going pulse with a low level of +0.4 V and a high level of +2.4 V (TTL limit levels).

(4) Press EXT ARM .

(5) Verify that the instrument is not counting.

(6) Trigger the pulse generator to obtain a single pulse output.

(7) Verify that the display indicates 10.0000000 MHz ± 0.0000001 MHz and that the instrument is not continuously gating.

(8) Press [EXT ARM] .

(9) Disconnect the test equipment.

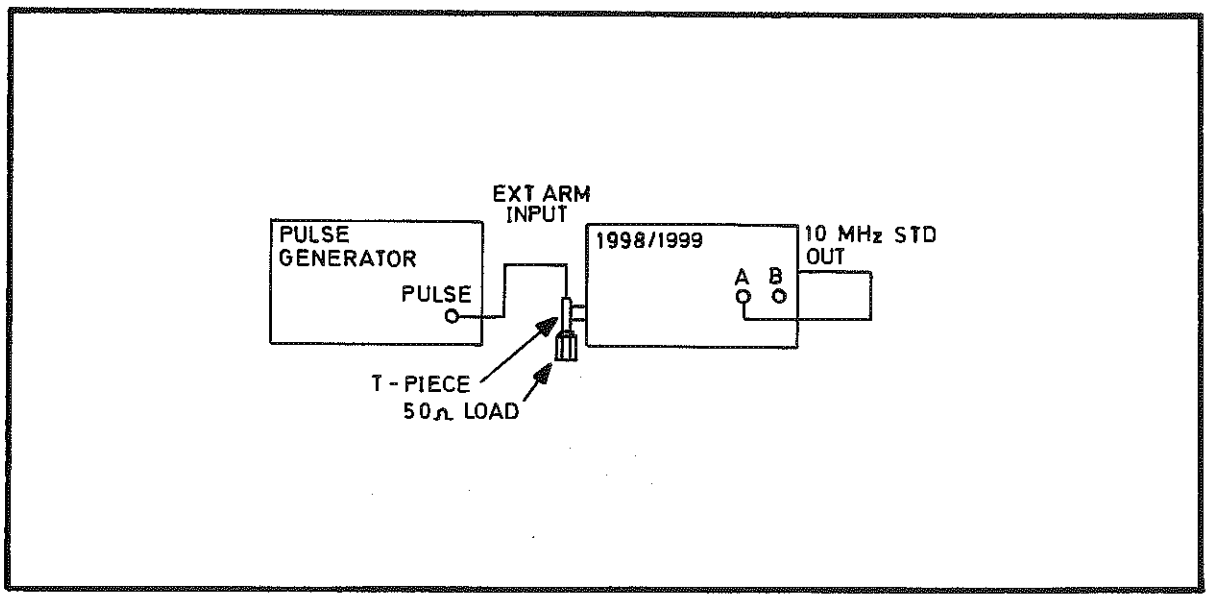


Fig 7.27 Connections for External Arming PVP

Internal Frequency Standard PVP

91 Test equipment required:

Item	Table 7.1 Item No
Frequency Standard	4
Coaxial Lead	7

92 (1) Select FREQ A and 100 ms gate time. If the Option 04B (9423) frequency standard is fitted, press the RESOLUTION key to give 1 s gate time.

(2) Connect the 10 MHz STD OUTPUT socket to the A channel input, using the coaxial lead.

(3) Press [NULL] .

(4) Disconnect the signal from the A channel input.

(5) Connect the frequency standard as shown in Fig 7.28

(6) Verify that the value displayed is within the limits shown in Table 7.10.

(7) Press [NULL] . Disconnect the test equipment.

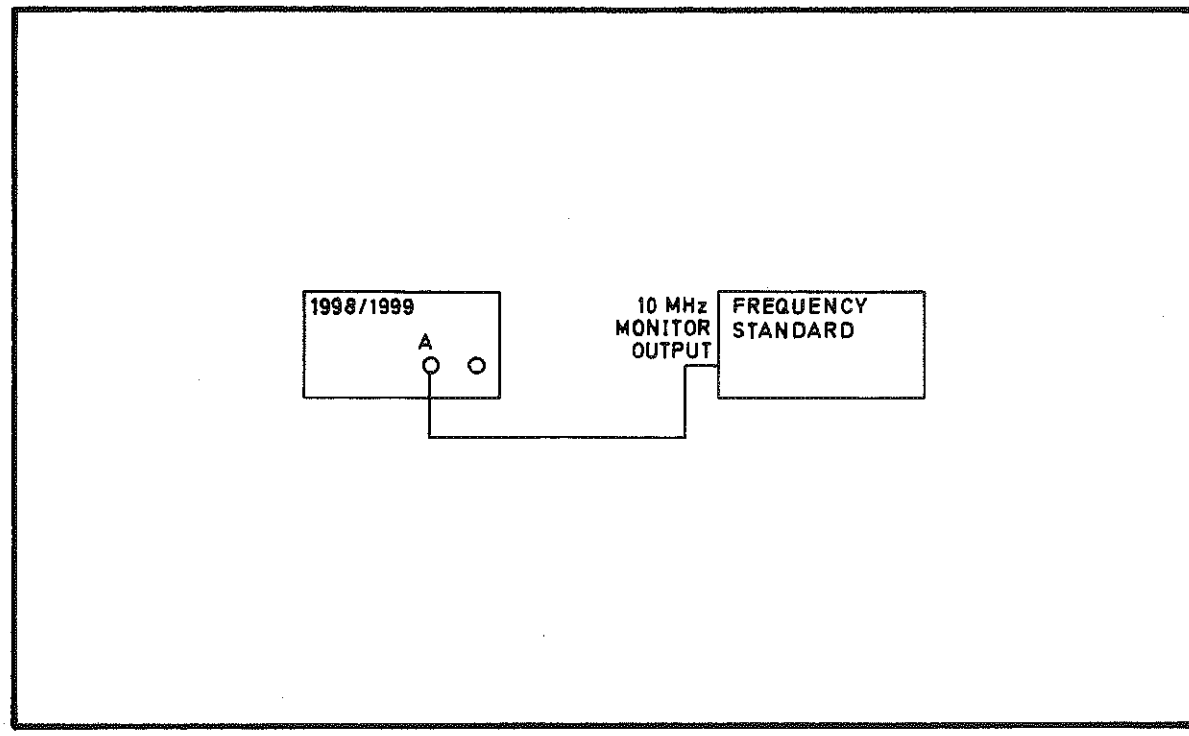


Fig 7.28 Connections for Internal Frequency Standard PVP

TABLE 7.10

Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Standard Oscillator	±10.0 Hz	10 parts in 10^7
Option 04T	±2.0 Hz	2 parts in 10^7
Option 04A (9444)	±0.2 Hz	2 parts in 10^8
Option 04B (9423)	±0.02 Hz	2 parts in 10^9

Gate Output PVP

93 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope	2
Coaxial Lead	7

94 (1) Connect the 10 MHz STD OUTPUT socket to the A channel input, using the coaxial lead.

(2) Select a 1 second gate time. Verify that the 1998/1999 indicates 10.00000000 MHz ± 0.00000001 MHz

(3) Switch the oscilloscope input to DC coupling. Monitor the GATE OUTPUT terminal on the rear panel. Verify that the voltage is +2.4 V when the GATE indicator is on, and +0.4 V when the GATE indicator is off.

(4) Switch off the 1998/1999. Switch off and disconnect the test equipment.

PARTS LIST

FRONT AND REAR PANEL ASSEMBLIES

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
REAR PANEL ASSEMBLY					
		Feedthrough terminals for gate output			24-3547
FRONT PANEL ASSEMBLY (1998)					
INPUT B		BNC to SMB socket, fused			17-1038
		Fuselink for 17-1038 (pack of 5)			11-1718
FRONT PANEL ASSEMBLY (1999)					
INPUT B		N socket			17-1500

PARTS LIST

CHANNEL B ASSEMBLY 19-1142

Fig 3

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors	Ω		W		
R1		Not Used			
R2		Not Used			
R3	10k	Chip	0.125	5	20-5768
R4	10k	Chip	0.125	5	20-5768
R5	150	Chip	1	5	20-5841
R6	39	Chip	1	5	20-5837
R7	330	Chip	0.125	5	20-5787
R8	150	Chip	0.125	5	20-5783
R9	270	Chip	0.125	5	20-5786
R10	100	Chip	0.125	5	20-5764
R11	270	Chip	0.125	5	20-5786
R12	10	Chip	0.125	5	20-5771
R13	33	Chip	0.125	5	20-5776
R14	330	Chip	0.125	5	20-5787
R15	270	Chip	0.125	5	20-5786
R16	390	Chip	0.125	5	20-5788
R17		Not Used			
R18	10	Chip	0.125	5	20-5776
R19	33	Chip	0.125	5	20-5776
R20	330	Chip	0.125	5	20-5787
R21	180	Chip	0.125	5	20-5784
R22	180	Chip	0.125	5	20-5784
R23	390	Chip	0.125	5	20-5788
R24	10	Chip	0.125	5	20-5771
R25	33	Chip	0.125	5	20-5776
R26	330	Chip	0.125	5	20-5787
R27	20k	Variable			20-7049
R28	390	Chip	0.125	5	20-5788
R29	100k	Chip	0.125	5	20-5813
R30	10	Chip	0.125	5	20-5771
R31	22	Chip	0.125	5	20-5774
R32	220	Chip	0.125	5	20-5785
R33	1.5k	Chip	0.125	5	20-5794
R34	1.5k	Chip	0.125	5	20-5794
R35	56k	Chip	0.125	5	20-5810

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	10	Chip	0.125	5	20-5771
R37	56	Chip	0.125	5	20-5779
R38	56k	Chip	0.125	5	20-5810
R39	1M	Chip	0.125	5	20-5770
R40		Not Used			
R41	4.7k	Chip	0.125	5	20-5799
R42	4.7k	Chip	0.125	5	20-5799
R43		Not Used			
R44	1k	Chip	0.125	5	20-5792
R45	150	Chip	0.125	5	20-5783
R46	27	Chip	0.125	5	20-5775
R47	27	Chip	0.125	5	20-5775
R48	27	Chip	0.125	5	20-5775
R49	27	Chip	0.125	5	20-5775
R50	470	Chip	0.125	5	20-5765
R51		Not Used			
R52	6.8k	Chip	0.125	5	20-5801
R53	3.3k	Chip	0.125	5	20-5797
R54	1k	Chip	0.125	5	20-5792
R55	1k	Chip	0.125	5	20-5792
R56	680	Chip	0.125	5	20-5790
R57	2.7k	Chip	0.125	5	20-5766
R58	3.3k	Chip	0.125	5	20-5797
R59	1k	Chip	0.125	5	20-5792
R60	1k	Chip	0.125	5	20-5792
R61	1k	Chip	0.125	5	20-5792
R62	1k	Chip	0.125	5	20-5792
R63		Not Used			
R64		Not Used			
R65		Not Used			
R66	150	Chip	0.125	5	20-5783
R67		Not Used			
R68	1M	Chip	0.125	5	20-5770
R69	1M	Chip	0.125	5	20-5770
R70	10	Chip	0.125	5	20-5771
R71	10	Chip	0.125	5	20-5771

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	10n	Chip	50	20	21-1801
C5	10n	Chip	50	20	21-1801
C6	10n	Chip	50	20	21-1801
C7	3.3p	Chip	50	0.25p	21-1781
C8	10n	Chip	50	20	21-1801
C9	10n	Chip	50	20	21-1801
C10	10n	Chip	50	20	21-1801
C11	3.3p	Chip	50	0.25p	21-1781
C12	10n	Chip	50	20	21-1801
C13	10n	Chip	50	20	21-1801
C14	3.3p	Chip	50	0.25p	21-1781
C15	10n	Chip	50	20	21-1801
C16	47µ	Electrolytic	25	-10+50	21-0615
C17	10n	Chip	50	20	21-1801
C18	10n	Chip	50	20	21-1801
C19	4.7p	Chip	50	0.25p	21-1783
C20		Not Used			
C21	10n	Chip	50	20	21-1801
C22	3.3p	Chip	50	0.25p	21-1781
C23	12p	Chip	50	5	21-1799
C24	10n	Chip	50	20	21-1801
C25	10n	Chip	50	20	21-1801
C26	1n	Chip	50	20	21-1800
C27	47µ	Electrolytic	25	-10+50	21-0615
C28	10n	Chip	50	20	21-1801
C29	10n	Chip	50	20	21-1801
C30	10n	Chip	50	20	21-1801
C31	10n	Chip	50	20	21-1801
C32	10n	Chip	50	20	21-1801
C33	5.6p	Chip	50	0.25p	21-1784
C34	6.8p	Chip	50	0.25p	21-1785
C35	6.8p	Chip	50	0.25p	21.1785

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C36	6.8p	Chip	50	0.25p	21-1785
C37	47p	Chip	50	5	21-1795
C38	10n	Chip	50	20	21-1801
C39	10n	Chip	50	20	21-1801
C40	3.3p	Chip	50	0.25p	21-1781
C41	3.3p	Chip	50	0.25p	21-1781
C42	5.6p	Chip	50	0.25p	21-1784
C43	10n	Chip	50	20	21-1801
C44	47µ	Electrolytic	25	-10+50	21-0615
C45	47µ	Electrolytic	6.3	20	21-0704
C46	3.9p	Chip	50	0.25	21-1782
C47	10n	Chip	50	20	21-1801
C48	10n	Chip	50	20	21-1801
C49	3.3p	Chip	50	0.25p	21-1781
C50	3.3p	Chip	50	0.25p	21-1781
C51	15p	Chip	50	5	21-1789
C52	15p	Chip	50	5	21-1789
C53	100n	Ceramic	50	20	21-1708
Diodes					
D1		Schottky (5082.2835)			22-1086
D2		PIN (5082.3379)			22-1058
D3		Schottky (5082.2835)			22-1086
D4		Not Used			
D5		Schottky (5082.2835)			22-1086
D6		Schottky (5082.2835)			22.1086
D7		PIN (5082.3379)			22-1058
D8		Hot Carrier (5082.2800)			22-1068
D9		Hot Carrier (5082.2800)			22-1068
D10		Voltage Regulator (BZX79C9V1)			22-1814
D11		Voltage Regulator (BZX79C9V1)			22-1814
D12		Silicon (IN4149)			22-1029
Transistors					
Q1		BFR90			22-6123
Q2		BFR90			22-6123
Q3		BFR90			22-6123
Q4		HXTR3101			22-6155

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits					
IC1		LM339			22-4249
IC2		MC10116			22-4528
IC3		SP4730/SP4731			22-4694
IC4		74LS00			22-4531
Inductors					
L1		Coil Assembly			17-3240
Connectors					
SK7		Connector, 30-way			23-5173
		Coaxial Cable Assembly			10-2891

PARTS LIST

OSCILLATOR ASSEMBLY 19-1147

Fig 5

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors	F		V		
C1	100n	Ceramic	50	20	21-1708
Connector					
SK14		Connector, 5-way			23-5166
Oscillator					
	10MHz	Crystal oscillator			23-9134

PARTS LIST

MOTHERBOARD ASSEMBLY 19-1160

Figs 7, 8 and 9

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors	Ω		W		
R1		Not Used			
R2		Not Used			
R3	100	Metal Oxide	2	5	20-4674
R4		Not Used			
R5	100	Metal Oxide	2	5	20-4674
R6	33	Chip	0.125	5	20-5776
R7	953k	Metal Film	½	1	20-7546
R8	53.6k	Metal Film	¼	1	20-7548
R9	1M	Metal Film	¼	1	20-4995
R10	100	Metal Oxide	1	5	20-4673
R11	10	Chip	0.125	5	20-5771
R12	10k	Chip	0.125	5	20-5768
R13	10k	Chip	0.125	5	20-5768
R14	33	Chip	0.125	5	20-5776
R15	150k	Chip	0.125	5	20-5860
R16	150k	Chip	0.125	5	20-5860
R17	82k	Chip	0.125	5	20-5812
R18	470	Chip	0.125	5	20-5765
R19	10k	Variable		20	20-7071
R20	150k	Chip	0.125	5	20-5860
R21	82k	Chip	0.125	5	20-5812
R22	150k	Chip	0.125	5	20-5860
R23	470	Chip	0.125	5	20-5765
R24	10k	Variable		20	20-7071
R25	10k	Chip	0.125	5	20-5768
R26	68	Chip	0.125	5	20-5780
R27	10	Chip	0.125	5	20-5771
R28	330	Chip	0.125	5	20-5787
R29	330	Chip	0.125	5	20-5787
R30	330	Chip	0.125	5	20-5787
R31	330	Chip	0.125	5	20-5787
R32	330	Chip	0.125	5	20-5787
R33	1.5k	Chip	0.125	5	20-5794
R34	220	Chip	0.125	5	20-5785
R35	10k	Chip	0.125	5	20-5768

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	10k	Chip	0.125	5	20-5768
R37	10k	Chip	0.125	5	20-5768
R38	10	Chip	0.125	5	20-5771
R39	330	Chip	0.125	5	20-5787
R40		Not Used			
R41	47	Chip	0.125	5	20-5778
R42	68	Chip	0.125	5	20-5780
R43	1k	Chip	0.125	5	20-5792
R44	1k	Chip	0.125	5	20-5792
R45	10k	Chip	0.125	5	20-5768
R46	6.8k	Chip	0.125	5	20-5801
R47	100k	Chip	0.125	5	20-5813
R48	100k	Chip	0.125	5	20-5813
R49	4.7k	Chip	0.125	5	20-5799
R50	4.7k	Chip	0.125	5	20-5799
R51	10k	Chip	0.125	5	20-5768
R52	10k	Chip	0.125	5	20-5768
R53	4.7k	Chip	0.125	5	20-5799
R54	2.2k	Chip	0.125	5	20-5796
R55	68	Chip	0.125	5	20-5780
R56	10k	Chip	0.125	5	20-5768
R57	4.7k	Chip	0.125	5	20-5799
R58	10k	Chip	0.125	5	20-5768
R59	10k	Chip	0.125	5	20-5768
R60	10k	Chip	0.125	5	20-5768
R61	100k	Chip	0.125	5	20-5813
R62	1k	Chip	0.125	5	20-5792
R63	330	Chip	0.125	5	20-5787
R64	10k	Chip	0.125	5	20-5768
R65	10k	Chip	0.125	5	20-5768
R66	1k	Chip	0.125	5	20-5792
R67	1k	Chip	0.125	5	20-5792
R68	1k	Chip	0.125	5	20-5792
R69	1k	Chip	0.125	5	20-5792
R70	4.7k	Chip	0.125	5	20-5799
R71	1k	Chip	0.125	5	20-5792
R72	1k	Chip	0.125	5	20-5792
R73	150k	Chip	0.125	5	20-5860
R74	4.7k	Chip	0.125	5	20-5799
R75	470	Chip	0.125	5	20-5765

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R76	1k	Chip	0.125	5	20-5792
R77	470	Chip	0.125	5	20-5765
R78	1k	Chip	0.125	5	20-5792
R79	1k	Chip	0.125	5	20-5792
R80	1k	Chip	0.125	5	20-5792
R81	1.5k	Chip	0.125	5	20-5794
R82	5 x 10k	SIL Array			20-5562
R83	4.7k	Chi	0.125	5	20-5799
R84	2.2k	Chip	0.125	5	20-5796
R85	1k	Chip	0.125	5	20-5792
R86	1k	Chip	0.125	5	20-5792
R87	1k	Chip	0.125	5	20-5792
R88	220	Chip	0.125	5	20-5785
R89	470	Chip	0.125	5	20-5765
R90	120	Carbon Film	¼	5	20-2121
R91	120	Carbon Film	¼	5	20-2121
R92	120	Carbon Film	¼	5	20-2121
R93		SIL Array (Custom Built)			20-5556
R94	10k	Chip	0.125	5	20-5768
R95	1.5k	Chip	0.125	5	20-5794
R96	18	Chip	0.125	5	20-5763
R97	68	Chip	0.125	5	20-5780
R98	82k	Chip	0.125	5	20-5812
R99	1k	Chip	0.125	5	20-5792
R100	10k	Chip	0.125	5	20-5768
R101	4.7k	Chip	0.125	5	20-5799
R102	10k	Chip	0.125	5	20-5768
R103	12k	Chip	0.125	5	20-5802
R104	470	Chip	0.125	5	20-5765
R105	4.7k	Chip	0.125	5	20-5799
R106	470	Chip	0.125	5	20-5765
R107	10	Chip	0.125	5	20-5771
R108	10k	Chip	0.125	5	20-5768
R109	10k	Chip	0.125	5	20-5768
R110	2.2k	Chip	0.125	5	20-5796
R111	47k	Chip	0.125	5	20-5809
R112	10	Chip	0.125	5	20-5771

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	10n	Chip	50	10	21-1801
C2	10n	Chip	50	10	21-1801
C3	47µ	Electrolytic	25	20	21-0789
C4	10n	Chip	50	10	21-1801
C5	10n	Chip	50	10	21-1801
C6	10n	Chip	50	10	21-1801
C7	20n	Chip	400	10	21-1847
C8	6.8p	Chip	400	±0.25p	21-1859
C9	120p	Chip	50	10	21-1845
C10	10n	Chip	50	10	21-1801
C11	10n	Chip	50	10	21-1801
C12		Not Used			
C13		Not Used			
C14	33n	Chip	50	10	21-1808
C15	10n	Chip	50	10	21-1801
C16	10n	Chip	50	10	21-1801
C17	33n	Chip	50	10	21-1808
C18	47µ	Electrolytic	25	20	21-0789
C19	47µ	Electrolytic	25	20	21-0789
C20	10n	Chip	50	10	21-1801
C21	10n	Chip	50	10	21-1801
C22	10n	Chip	50	10	21-1801
C23	10n	Chip	50	10	21-1801
C24	10n	Chip	50	10	21-1801
C25	10n	Chip	50	10	21-1801
C26	10n	Chip	50	10	21-1801
C27	10n	Chip	50	10	21-1801
C28	47µ	Electrolytic	25	20	21-0789
C29	10n	Chip	50	10	21-1801
C30	10n	Chip	50	10	21-1801
C31	33n	Chip	50	10	21-1808
C32	47µ	Electrolytic	25	20	21-0789
C33	10n	Chip	50	10	21-1801
C34	47µ	Electrolytic	25	20	21-0789
C35	10n	Chip	50	10	21-1801

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C36	10n	Chip	50	10	21-1801
C37	1µ	Electrolytic	50	20	21-0779
C38	1n	Chip	50	20	21-1800
C39	33n	Chip	50	10	21-1808
C40	47µ	Electrolytic	25	20	21-0789
C41	1µ	Electrolytic	50	20	21-0779
C42	33n	Chip	50	10	21-1808
C43	33n	Chip	50	10	21-1808
C44	33n	Chip	50	10	21-1808
C45	20n	Chip	400	10	21-1847
C46	10n	Chip	50	10	21-1801
C47	47n	Polypropylene	250	20	21-7003
C48	10n	Chip	50	10	21-1801
C49	2.5n	Polypropylene	250	20	21-7002
C50	2.5n	Polypropylene	250	20	21-7002
C51	33n	Chip	50	10	21-1808
C52	33n	Chip	50	10	21-1808
C53	47µ	Electrolytic	25	20	21-0789
C54	10n	Chip	50	10	21-1801
C55	10n	Chip	50	10	21-1801
C56	33n	Chip	50	10	21-1808
C57	680µ	Electrolytic	25	20	21-0797
C58	10000µ	Electrolytic	16	-10+30	21-0683
C59	4700µ	Electrolytic	16	-10+30	21-0667
C60	47µ	Electrolytic	25	20	21-0789
C61	1µ	Electrolytic	50	20	21-0779
C62	120p	Chip	50	5	21-1845
C63	120p	Chip	50	5	21-1845
C64	120p	Chip	50	5	21-1845
C65	10µ	Electrolytic	16	20	21-0775
C66	10n	Chip	50	10	21-1801
C67	47µ	Electrolytic	25	20	21-0789
C68	47µ	Electrolytic	25	20	21-0789
C69	47µ	Electrolytic	25	20	21-0789
C70	33n	Chip	50	10	21-1808
C71	33n	Chip	50	10	21-1808
C72	120p	Chip	50	5	21-1845
C73	6.8p	Chip	50	0.25p	21-1785
C74	1µ	Electrolytic	50	20	21-0779

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Diodes					
D1		Not Used			
D2		Silicon (1N4150)			22-1100
D3		Silicon (1N4150)			22-1100
D4		Silicon (1N4150)			22-1100
D5		Silicon (1N4150)			22-1100
D6		Silicon (1N4150)			22-1100
D7		Silicon (1N4150)			22-1100
D8		Silicon (1N4150)			22-1100
D9		Silicon (1N4150)			22-1100
D10		Silicon (1N4150)			22-1100
D11		Bridge Rectifier (VH248)			22-1662
D12		Silicon (1N4002)			22-1602
D13		Silicon (1N4002)			22-1602
D14		Not Used			
D15		Voltage Regulator (BZX79B5V1)			22-1857
Transistors					
Q1		Not Used			
Q2		2N3906			22-6008
Q3		2N3906			22-6008
Q4		2N3904			22-6007
Q5		CA3083			22-4216
Q6		2N3906			22-6008
Q7		2N3906			22-6008
Q8		2N3904			22-6007
Q9		2N3904			22-6007
Q10		2N3904			22-6007
Q11		BDT92			22-6153
Q12		2N3904			22-6007
Q13		BDT92			22-6153
Q14		2N3904			22-6007
Q15		2N3906			22-6008
Q16		BDT91			22-6152
Q17		2N3904			22-6007
Q18		BDT92			22-6153

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits					
IC1		74HCT373			22-4808
IC2		Programmed 2764			22-8574
IC3		74LS32			22-4578
IC4		40106			22-4756
IC5		MC146805E2			22-8307
NOTE: When ordering a replacement for IC2, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.					
IC6		74LS74			22-4534
IC7		4011			22-4700
IC8		MC3403			22-4262
IC9		MCC1 (Custom Built)			22-8403
IC10		74LS04			22-4533
IC11		74LS373			22-4585
IC12		74HCT373			22-4808
IC13		74HCT244			22-4807
IC14		74LS138			22-4587
IC15		74LS10			22-4557
IC16		MC10116			22-4528
IC17		MC10116			22-4528
IC18		MCC 2 (Custom Built)			22-8404
IC19		MC10231			22-4542
IC20		SP9687DG			22-4686
H1		TEC (Custom Built)			17-1034
Inductors	H				
L1	10µ	Choke			23-7155
L2	100µ	Choke			23-7213
L3	100µ	Choke			23-7213
L4	100µ	Choke			23-7213
L5	1µ	Choke			23-7192
L6		Not Used			
L7		Choke			17-3166
L8		Choke			17-3166
L9	100µ	Choke			23-7213
L10	40µ	Choke			23-7217
L11	40µ	Choke			23-7217

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL1		Plug, 2x7-way			23-5162
PL2		Plug, 2x7-way			23-5162
PL3		Not Used			
PL4		Not Used			
PL5		Not Used			
PL6		Not Used			
PL7		Plug, 30-way			23-5174
PL8		Not Used			
PL9		Not Used			
PL10		Not Used			
PL11		Not Used			
PL12		Not Used			
PL13		Not Used			
PL14		Plug, 5-way			23-5164
PL15		Not Used			
PL16		Plug, 10-way			23-5165
PL17		Plug, 5-way			23-5164
PL18		Not Used			
PL19		Plug 2x2-way			23-5161
PL20		Plug, 2x2-way			23-5161
PL21		Plug, 2x10-way			23-5168
PL23		Plug, 10-way			23-5165
SK1		Not Used			
SK2		Not Used			
SK3		Not Used			
SK4		IC Socket, 28-way			23-3290
SK5		Socket, BNC			17-1043
SK6		Not Used			
SK7		Not Used			
SK8		Socket, 6-way			23-5177
LK1					23-9124
LK3					23-9124
LK5					23-5180
LK6					23-5180
LK7					23-9124
		AC Power Plug, PCB mounting			23-3429

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Miscellaneous					
FS1		Fuselink 1¼ in x ¼ in 250mAT (193 V to 253 V)			23-0056
		Fuselink 1¼ in x ¼ in 500mAT (90 V to 127 V)			23-0052
		Fuseholder for FS1			23-0062
		Top for 23-0062			23-0063
		IC Socket, 28-way			23-3290
		IC Socket, 40-way			23-3297
S1		Mains Switch			23-4124
		Button for 23-4124			15-0674
		Control Rod for 23-4124			15-0693
T1		Mains Transformer			17-4102
RLA		Not Used			
RLB		Relay, Reed			23-7529
RLC		Relay, Reed DIL			23-7530
RLD		Relay, Reed			23-7528

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Miscellaneous					
FS1		Fuselink 1¼ in x ¼ in 250mAT (193 V to 253 V)			23-0056
		Fuselink 1¼ in x ¼ in 500mAT (90 V to 127 V)			23-0052
		Fuseholder for FS1			23-0062
		Top for 23-0062			23-0063
		IC Socket, 28-way			23-3290
		IC Socket, 40-way			23-3297
S1		Mains Switch			23-4124
		Button for 23-4124			15-0674
		Control Rod for 23-4124			15-0693
T1		Mains Transformer			17-4102
RLA		Not Used			
RLB		Relay, Reed			23-7529
RLC		Relay, Reed DIL			23-7530
RLD		Relay, Reed			23-7528

PARTS LIST

DISPLAY ASSEMBLY 19-1163

Fig 11

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistor	Ω		W		
R1	9X10k	SIL Array			20-5521
Capacitors	F		V		
C1	100n	Ceramic	50	20	21-1708
C2	4.7µ	Electrolytic	50	20	21-0750
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
Diodes					
LP1		LED, red			26-5026
LP2		LED, red			26-5026
LP3		LED, red			26-5026
LP4		LED, red			26-5026
LP5		LED, red			26-5026
LP6		LED, red			26-5026
LP7		LED, red			26-5026
LP8		LED, red			26-5026
LP9		LED, red			26-5026
LP10		LED, red			26-5026
LP11		LED, red			26-5026
LP12		LED, red			26-5026
LP13		LED, red			26-5026
LP14		LED, red			26-5026
LP15		LED, red			26-5026
LP16		LED, red			26-5026
LP17		LED, red			26-5026
LP18		LED, red			26-5026
LP19		LED, red			26-5026
LP20		LED, red			26-5026

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
LP21		LED, red			26-5026
LP22		LED, red			26-5026
LP23		LED, red			26-5026
LP24		LED, red			26-5026
LP25		LED, red			26-5026
LP26		LED, red			26-5026
LP27		LED, red			26-5026
LP28		LED, red			26-5026
LP29		LED, red			26-5026
LP30		LED, red			26-5026
LP31		LED, red			26-5026
LP32		LED, red			26-5026
Integrated Circuits					
IC1		74C922			22-4779
IC2		7218AIJI			22-4778
IC3		7218AIJI			22-4778
Displays					
DI1		Seven-segment display; double digit			26-1512
DI2		Seven-segment display; double digit			26-1512
DI3		Seven-segment display; double digit			26-1512
DI4		Seven-segment display; double digit			26-1512
DI5		Seven-segment display; double digit			26-1512
Miscellaneous					
S1-S14		Keyswitch, single-pole			23-4125
		Button, blue			15-0705
		Button, grey			15-0703
SK1		Socket, 14-way			23-5160
SK2		Socket, 14-way			23-5160

PARTS LIST

BNC MOUNTING BOARD 19-1206

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Sockets					
EXT STD INPUT		BNC socket, PCB mounting			23-3421
EXT ARM INPUT		BNC socket, PCB mounting			23-3421
10MHz STD OUTPUT		BNC socket, PCB mounting			23-3421
SK19		Connector 2 x 2 way			23-5159
SK20		Connector 2 x 2 way			23-5159

PARTS LIST

INPUT A AMPLIFIER ASSEMBLY 19-1237

Fig 13

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors	Ω		W		
R1	12	Chip	0.125	5	20-5772
R2	1k	Chip	0.125	5	20-5792
R3	680	Chip	0.125	5	20-5790
R4	500	Variable			20-7083
R5	120	Chip	0.125	5	20-5782
R6	12	Chip	0.125	5	20-5772
R7	470	Variable			20-7114
R8	12	Chip	0.125	5	20-5772
R9	47	Chip	0.125	5	20-5778
R10	12	Chip	0.125	5	20-5772
R11	1k	Chip	0.125	5	20-5792
R12	100	Chip	0.125	5	20-5764
R13	220	Chip	0.125	5	20-5785
R14	12	Chip	0.125	5	20-5772
R15	1k	Chip	0.125	5	20-5792
R16	1k	Chip	0.125	5	20-5792
R17	220	Chip	0.125	5	20-5785
Capacitors	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	47µ	Electrolytic	25	20	21-0789
C5	100µ	Electrolytic	6.3	20	21-0774
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	4.7p	Chip	50	±0.25p	21-1783
C9	8.2p	Chip	50	±0.25p	21-1786
C10	10n	Chip	50	20	21-1801
C11	100µ	Electrolytic	6.3	20	21-0774
C12	10n	Chip	50	20	21-1801
C13	10n	Chip	50	20	21-1801
C14	100µ	Electrolytic	6.3	20	21-0774

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
Q1		BF256B			22-6211
Q2		BFS17			22-6206
Q3		BFS17			22-6206
Q4		BFS17			22-6206
Q5		BFS17			22-6206
Q6		BFS17			22-6206
Q7		3904			22-6197
Connectors					
SK23		Socket, 10-way			23-5167
Miscellaneous					
		Cap			24-0519
		Knob			24-0520

PARTS LIST

CHANNEL B ASSEMBLY 19-1300

Fig 15

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors			W		
R1	150	Chip	0.125	5	20-5783
R2	150	Chip	0.125	5	20-5783
R3	330	Chip	0.125	5	20-5787
R4	390	Chip	0.125	5	20-5788
R5	220	Chip	0.125	5	20-5785
R6	150	Chip	0.125	5	20-5783
R7	270	Chip	0.125	5	20-5786
R8	270	Chip	0.125	5	20-5786
R9	18	Chip	0.125	5	20-5763
R10	270	Chip	0.125	5	20-5786
R11	100	Chip	0.125	5	20-5764
R12	1.5k	Chip	0.125	5	20-5794
R13	180k	Chip	0.125	5	20-5861
R14	2.2k	Chip	0.125	5	20-5796
R15	220	Chip	0.125	5	20-5785
R16	1.5k	Chip	0.125	5	20-5794
R17	220	Chip	0.125	5	20-5785
R18	390	Chip	0.125	5	20-5788
R19	8.2k	Chip	0.125	5	20-5767
R20	390	Chip	0.125	5	20-5788
R21	3.9k	Chip	0.125	5	20-5798
R22	1.8k	Chip	0.125	5	20-5795
R23	82k	Chip	0.125	5	20-5812
R24	330	Chip	0.125	5	20-5787
R25	10k	Chip	0.125	5	20-5768
R26	2.7k	Chip	0.125	5	20-5766
R27	390	Chip	0.125	5	20-5788
R28	27	Chip	0.125	5	20-5775
R29	3.9k	Chip	0.125	5	20-5798
R30	1k	Chip	0.125	5	20-5792
R31	680	Chip	0.125	5	20-5790
R32	1.8k	Chip	0.125	5	20-5795
R33	270	Chip	0.125	5	20-5786
R34	1k	Chip	0.125	5	20-5792
R35	680	Chip	0.125	5	20-5790

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	5k	Variable		20	20-7117
R37	3.9k	Chip	0.125	5	20-5798
R38	6.8k	Chip	0.125	5	20-5801
R39	5k	Variable		20	20-7117
R40	270	Chip	0.125	5	20-5786
R41	12k	Chip	0.125	5	20-5802
R42	10k	Chip	0.125	5	20-5768
R43	1M	Chip	0.125	5	20-5770
R44	1M	Chip	0.125	5	20-5770
R45	1k	Chip	0.125	5	20-5792
R46	270	Chip	0.125	5	20-5786
R47	330	Chip	0.125	5	20-5787
R48	1k	Chip	0.125	5	20-5792
R49	270	Chip	0.125	5	20-5786
R50	330	Chip	0.125	5	20-5787
R51	1k	Chip	0.125	5	20-5792
R52	270	Chip	0.125	5	20-5786
R53	330	Chip	0.125	5	20-5787
R54	1k	Chip	0.125	5	20-5792
R55	270	Chip	0.125	5	20-5786
R56	330	Chip	0.125	5	20-5787
R57	560k	Chip	0.125	5	20-5817
R58	1k	Chip	0.125	5	20-5792
R59	100	Chip	0.125	5	20-5764
R60	2.7k	Chip	0.125	5	20-5766
R61	1k	Chip	0.125	5	20-5792
R62	330	Chip	0.125	5	20-5787
R63	330	Chip	0.125	5	20-5787
R64	180	Chip	0.125	5	20-5784
R65	180	Chip	0.125	5	20-5784
R66	220	Chip	0.125	5	20-5785
R67	220	Chip	0.125	5	20-5785
R68	220	Chip	0.125	5	20-5785
R69	180	Chip	0.125	5	20-5784
R70	1k	Chip	0.125	5	20-5792

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R71	5k	Variable		20	20-7117
R72	22k	Chip	0.125	5	20-5805
R73	22k	Chip	0.125	5	20-5805
R74	3.3k	Chip	0.125	5	20-5797
R75	3.9k	Chip	0.125	5	20-5798
R76	6.8k	Chip	0.125	5	20-5801
R77	330k	Chip	0.125	5	20-5816
R78	220k	Chip	0.125	5	20-5829
R79	68k	Chip	0.125	5	20-5811
R80	1k	Chip	0.125	5	20-5792
R81	1k	Chip	0.125	5	20-5792
R82	220	Chip	0.125	5	20-5785
R83	1k	Chip	0.125	5	20-5792
R84	4.7k	Chip	0.125	5	20-5799
R85	4.7k	Chip	0.125	5	20-5799
R86	4.7	Chip	0.125	5	20-5866
R87	680	Chip	0.125	5	20-5790
R88	2.7k	Chip	0.125	5	20-5766
R89	3.3k	Chip	0.125	5	20-5797
R90	1k	Chip	0.125	5	20-5792
R91	1k	Chip	0.125	5	20-5792
R92	1k	Chip	0.125	5	20-5792
R93	1k	Chip	0.125	5	20-5792
R94	1k	Chip	0.125	5	20-5792
R95	12k	Chip	0.125	5	20-5802
Capacitors			V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	390p	Chip	50	5	21-1799
C5	220p	Chip	50	5	21-1838
C6	0.6p	Porcelain Chip	50	0.1p	21-1863
C7	10µ	Electrolytic	25	+50-20	21-0798
C8	4.7p	Chip	50	0.25p	21-1783
C9	1n	Chip	50	20	21-1800
C10	220p	Chip	50	5	21-1838

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C11	10n	Chip	50	20	21-1801
C12	390p	Chip	50	5	21-1799
C13	10n	Chip	50	20	21-1801
C14	1n	Chip	50	20	21-1800
C15	10µ	Electrolytic	25	+50-20	21-0798
C16	10n	Chip	50	20	21-1801
C17	100n	Ceramic	50	20	21-1708
C18	1n	Chip	50	20	21-1800
C19	220p	Chip	50	5	21-1838
C20	1n	Chip	50	20	21-1800
C21	220p	Chip	50	5	21-1838
C22	1n	Chip	50	20	21-1800
C23	220p	Chip	50	5	21-1838
C24	1n	Chip	50	20	21-1800
C25	2.7p	Porcelain Chip	50	0.25p	21-1864
C26	4.7p	Chip	50	0.25p	21-1783
C27	390p	Chip	50	5	21-1799
C28	220p	Chip	50	5	21-1838
C29	1n	Chip	50	20	21-1800
C30	220p	Chip	50	5	21-1838
C31	1n	Chip	50	20	21-1800
C32	1n	Chip	50	20	21-1800
C33	10n	Chip	50	20	21-1801
C34	10n	Chip	50	20	21-1801
C35	1n	Chip	50	20	21-1800
C36	15p	Chip	50	5	21-1789
C37	15p	Chip	50	5	21-1789
C38	10n	Chip	50	20	21-1801
C39	3.3p	Chip	50	0.25p	21-1781
C40	3.3p	Chip	50	0.25p	21-1781
C41	3.3p	Chip	50	0.25p	21-1781
C42	3.3p	Chip	50	0.25p	21-1781
C43	3.3p	Chip	50	0.25p	21-1781
C44	10n	Chip	50	20	21-1801
C45	3.3p	Chip	50	0.25p	21-1781
C46	3.3p	Chip	50	0.25p	21-1781
C47	390p	Chip	50	5	21-1799
C48	3.3p	Chip	50	0.25p	21-1781
C49	3.3p	Chip	50	0.25p	21-1781
C50	390p	Chip	50	5	21-1799

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C51	3.3p	Chip	50	0.25p	21-1781
C52	3.3p	Chip	50	0.25p	21-1781
C53	1n	Chip	50	20	21-1800
C54	10n	Chip	50	20	21-1801
Diodes					
D1		A2S220			22-1102
D2		ZC2811E			22-1092
D3		A2S220			22-1102
D4		ZC2811E			22-1092
D5		BAS16			22-1093
Transistor					
Q1		BCF33			22-6193
Q2		BCF33			22-6193
Q3		FMMT3906			22-6199
Q4		BCF33			22-6193
Q5		FMMT3906			22-6199
Q6		FMMT3906			22-6199
Q7		BCF33			22-6193
Q8		FMMT3906			22-6199
Q9		FMMT3906			22-6199
Q10		BCF33			22-6193
Q11		FMMT3906			22-6199
Q12		BCF33			22-6193
Integrated Circuits					
IC1		DAA5126			22-2011
IC2		MSA0735			22-4697
IC3		MSA0735			22-4697
IC4		MSA0735			22-4697
IC5		MSA0735			22-4697
IC6		74LS00			22-4531
IC7		LM339			22-4249
IC8		MSA0735			22-4697
IC9		UPB582C			22-4695
IC10		SP4730/SP4731			22-4694
IC11		MC10116			22-4528

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Inductors					
L1	33µ			10	23-7163
L2	1µ			10	23-7192
L3	1µ			10	23-7192
Connectors					
TP1		Connector Jack			23-3446
TP2		Header 3-Way			17-1502
SK7		Connector 30-Way			23-5186
		Coaxial Connector Assembly			10-3500
Miscellaneous					
FX1		Ferrite Bead			23-8055
FX2		Ferrite Bead			23-8055

PARTS LIST

GPIB ASSEMBLY 19-1146

Fig 17

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors	Ω		W		
R1	9x3.3k	SIL Array			20-5532
R2	56	Carbon Film	¼	5	20-2560
R3	9x3.3k	SIL Array			20-5532
R4	330	Carbon Film	¼	5	20-2331
R5	330	Carbon Film	¼	5	20-2331
R6	330	Carbon Film	¼	5	20-2331
R7	5x3.3k	SIL Array			20-5531
R8	18	Carbon Film	¼	5	20-2180
R9	56	Carbon Film	¼	5	20-2560
R10	9x100k	SIL Array			20-5522
R11	5x100k	SIL Array			20-5558
Capacitors	F		V		
C1	47µ	Electrolytic	25	20	21-0789
C2	100n	Ceramic	50	20	21-1708
C3	100n	Ceramic	50	20	21-1708
C4	100n	Ceramic	50	20	21-1708
C5	100n	Ceramic	50	20	21-1708
C6	100n	Ceramic	50	20	21-1708
C7	100n	Ceramic	50	20	21-1708
C8	100n	Ceramic	50	20	21-1708
C9	10n	Ceramic	25	-20+80	21-1545
C10	10n	Ceramic	25	-20+80	21-1545
Integrated Circuits					
IC1		74HCT374			22-4809
IC2		74HCT374			22-4809
IC3		74HCT138			22-4806
IC4		7407			22-4063
IC5		74LS125			22-4657

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
IC6		74HCT02			22-4801
IC7		74HCT00			22-4800
IC8		74HCT138			22-4806
IC9		MC146805			22-8307
IC10		Programmed ROM			22-8009
NOTE: When ordering a replacement for IC10, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.					
IC11		74HCT373			22-4808
IC12		68488			22-8305
IC13		4066			22-4761
IC14		75161			22-4284
IC15		75160			22-4283
IC16		74HCT74			22-4805
IC17		74HCT74			22-4805
IC18		74HCT00			22-4800
IC19		74HCT02			22-4801
IC20		74HCT32			22-4804
Miscellaneous					
		IC Socket, 28-way			23-3290
		IC Socket, 40-way			23-3297
		IC Socket, 14-way			23-3309
SK3		Connector, 24-way			23-3434
S1		Switch, 6-way, DIL			23-4102

PARTS LIST

REFERENCE FREQUENCY MULTIPLIER ASSEMBLY 19-1164

Fig 19

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
	Ω		W		
R1	220	Chip	0.125	5	20-5785
R2	10k	Chip	0.125	5	20-5768
R3	12k	Chip	0.125	5	20-5802
R4	1.8k	Chip	0.125	5	20-5795
R5	100k	Chip	0.125	5	20-5813
R6	560k	Chip	0.125	5	20-5817
R7	10k	Chip	0.125	5	20-5768
R8	2.2k	Chip	0.125	5	20-5796
R9	2.2k	Chip	0.125	5	20-5796
R10	560	Chip	0.125	5	20-5789
R11	1.8k	Chip	0.125	5	20-5795
R12	330	Chip	0.125	5	20-5787
R13	2.2k	Chip	0.125	5	20-5796
R14	10k	Chip	0.125	5	20-5768
R15	10k	Chip	0.125	5	20-5768
R16	820	Chip	0.125	5	20-5791
R17	56	Chip	0.125	5	20-5779
R18	330	Chip	0.125	5	20-5787
R19	1.8k	Chip	0.125	5	20-5795
R20	56	Chip	0.125	5	20-5779
R21	56	Chip	0.125	5	20-5779
R22	820	Chip	0.125	5	20-5791
R23	1.8k	Chip	0.125	5	20-5795
R24	1.8k	Chip	0.125	5	20-5795
R25	1.8k	Chip	0.125	5	20-5795
R26	1.8k	Chip	0.125	5	20-5795
R27	220	Chip	0.125	5	20-5785
R28	220	Chip	0.125	5	20-5785
R29	220	Chip	0.125	5	20-5785
R30	220	Chip	0.125	5	20-5785
R31	220	Chip	0.125	5	20-5785

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	33n	Chip	50	10	21-1808
C2	2-15p	Variable			21-6043
C3	220p	Chip	50	5	21-1838
C4	220p	Chip	50	5	21-1838
C5	33n	Chip	50	10	21-1808
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801
C9	10n	Chip	50	20	21-1801
C10	10n	Chip	50	20	21-1801
C11	10n	Chip	50	20	21-1801
C12	10n	Chip	50	20	21-1801
C13	33n	Chip	50	10	21-1801
C14	33n	Chip	50	10	21-1801
C15	10n	Chip	50	20	21-1801
Diodes					
D1		Varactor (MV1640)			22-1097
D2		Silicon (BAS16)			22-1093
D3		Voltage regulator (BZX84C4V7)			22-1882
D4		Silicon (BAV99)			22-1096
D5		Silicon (BAV99)			22-1096
Transistors					
Q1		3904			22-6197
Q2		3906			22-6199
Q3		3906			22-6199
Q4		3904			22-6197
Q5		3904			22-6197
Q6		3904			22-6197
Q7		3904			22-6197
Integrated Circuits					
IC1		Not Used			
IC2		741			22-4292
IC3		MC10102			22-4514
IC4		74LS132			22-4582

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
SK16		Socket, 5-way			23-5166
SK17		Socket, 10-way			23-5167
Transformer					
T1		Transformer to Racal-Dana specification			17-3226

PARTS LIST

OSCILLATOR ASSEMBLY 19-1208

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors	F		V		
C1	100n	Ceramic	50	20	21-1708
Connector					
SK14		Connector, 5-way			23-5166
Oscillator					
	10MHz	Oscillator, temperature compensated			23-9135

PARTS LIST

REFERENCE FREQUENCY DOUBLER ASSEMBLY 19-1238

Fig 22

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors	Ω		W		
R1	33	Chip	0.125	5	20-5776
R2	100	Chip	0.125	5	20-5764
R3	100	Chip	0.125	5	20-5764
R4	1k	Chip	0.125	5	20-5792
R5	470	Chip	0.125	5	20-5765
R6	470	Chip	0.125	5	20-5765
R7	1.5k	Chip	0.125	5	20-5794
R8	3.9k	Chip	0.125	5	20-5798
R9	3.8k	Chip	0.125	5	20-5798
R10	1.5k	Chip	0.125	5	20-5794
R11	1k	Chip	0.125	5	20-5792
R12	39k	Chip	0.125	5	20-5808
R13	15k	Chip	0.125	5	20-5803
R14	330k	Chip	0.125	5	20-5816
R15	10k	Chip	0.125	5	20-5768
R16	1k	Chip	0.125	5	20-5792
R17	3.9k	Chip	0.125	5	20-5798
R18	3.9k	Chip	0.125	5	20-5798
R19	100	Chip	0.125	5	20-5764
R20	1k	Chip	0.125	5	20-5792
Capacitors	F		V		
C1	10n	Chip	50	20	21-1801
C2	10n	Chip	50	20	21-1801
C3	10n	Chip	50	20	21-1801
C4	10n	Chip	50	20	21-1801
C5	10n	Chip	50	20	21-1801
C6	10n	Chip	50	20	21-1801
C7	10n	Chip	50	20	21-1801
C8	10n	Chip	50	20	21-1801

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
Transistors					
Q1		2N3906			22-6008
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3904			22-6007
Q5		2N3904			22-6007
Q6		2N3904			22-6007
Inductors	H				
L1	100µ	Choke		10	23-7213
T1		10.7 MHz IF Transformer			23-7149
T2		10.7 MHz IF Transformer			23-7149

PARTS LIST

BATTERY PACK 11-1625

Fig 23

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
CHASSIS COMPONENTS					
	Ω		W		
R1	5.6	Wire Wound	10	5	20-5081
		Battery Chassis Assy (complete with batteries B1 and B2)			11-1723
		Cableform			10-2906
FS2		Fuselink 1¼ in x ¼ in	3AT		23-0069
FS3		Fuselink 1¼ in x ¼ in	3AT		23-0069
BATTERY BOARD ASSEMBLY 19-1203					
Resistors					
	Ω		W		
R1	39	Carbon Film	¼	5	20-2390
R2	1M	Chip	0.125	5	20-5770
R3	4.7k	Chip	0.125	5	20-5799
R4	1M	Chip	0.125	5	20-5770
R5	56	Carbon Film	¼	5	20-2560
R6	10M	Carbon Film	¼	10	20-2106
R7	1M	Chip	0.125	5	20-5770
R8	560k	Chip	0.125	5	20-5817
R9	560k	Chip	0.125	5	20-5817
R10	50k	Variable			20-7086
R11	56k	Chip	0.125	5	20-5810
R12	1k	Chip	0.125	5	20-5792
R13	22k	Chip	0.125	5	20-5805
R14	1M	Chip	0.125	5	20-5770
R15	560k	Chip	0.125	5	20-5817

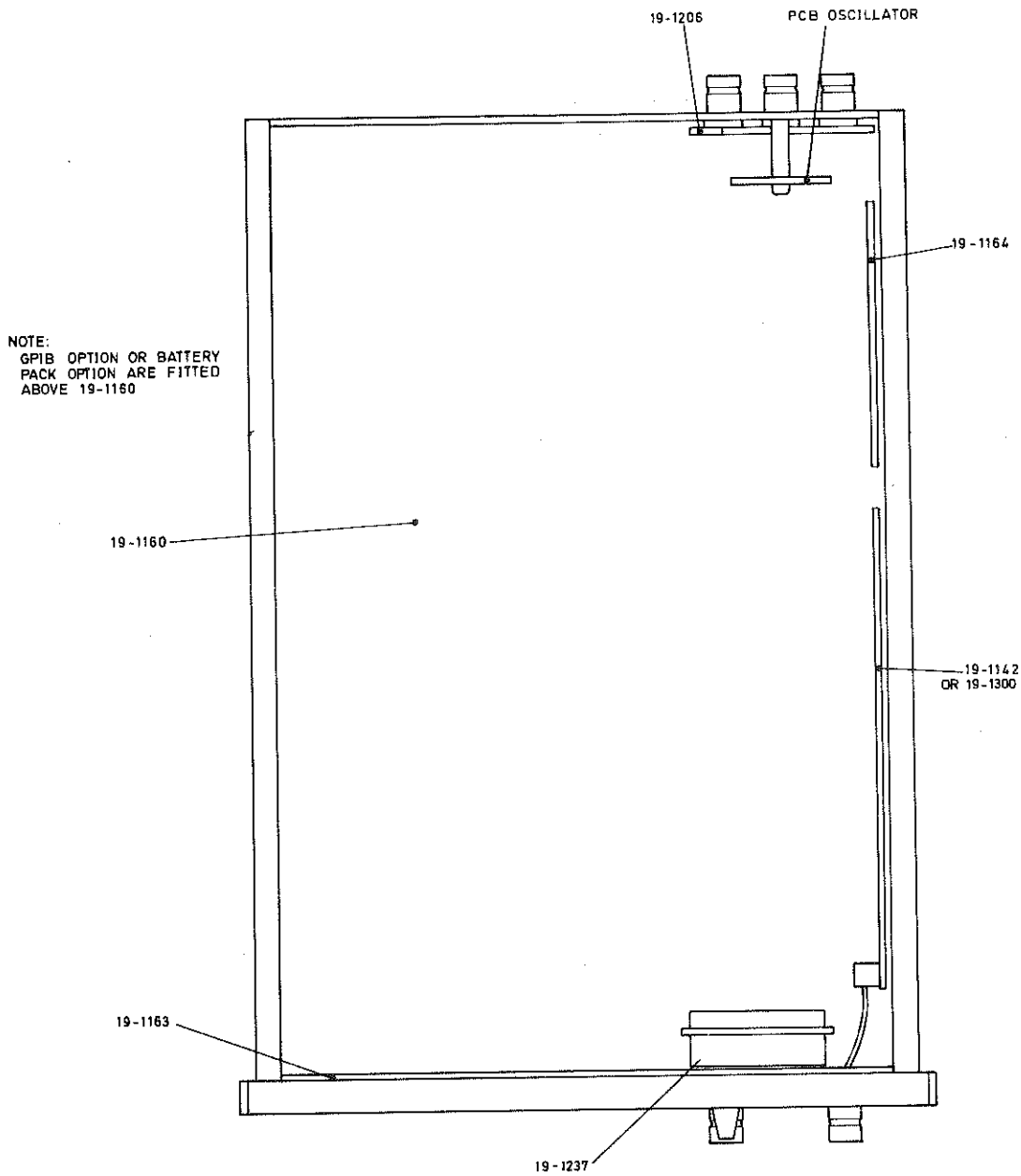
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R16	1M	Chip	0.125	5	20-5770
R17	10k	Chip	0.125	5	20-5768
R18	1M	Chip	0.125	5	20-5770
R19	1M	Chip	0.125	5	20-5770
R20	1M	Chip	0.125	5	20-5770
R21	10M	Carbon Film	¼	10	20-2106
R22	10k	Chip	0.125	5	20-5768
R23	10k	Chip	0.125	5	20-5768
R24	100k	Chip	0.125	5	20-5813
R25	56k	Chip	0.125	5	20-5810
R26	220	Chip	0.125	5	20-5785
R27	1k	Carbon Film	¼	5	20-2102
R28	20k	Variable			20-7116
R29	22k	Chip	0.125	5	20-5805
R30	22k	Chip	0.125	5	20-5805
R31	4.7k	Chip	0.125	5	20-5799
R32	4.7k	Chip	0.125	5	20-5799
R33	180	Carbon Film	¼	5	20-2181
R34	68	Carbon Film	½	5	20-3680
R35	180	Chip	0.125	5	20-5784
R36	50k	Variable			20-7086
R37	220k	Chip	0.125	5	20-5829
R38	10k	Chip	0.125	5	20-5768
R39	3.9k	Chip	0.125	5	20-5798
R40	560	Chip	0.125	5	20-5789
R41	39k	Chip	0.125	5	20-5808
R42	1k	Chip	0.125	5	20-5792
R43	27k	Chip	0.125	5	20-5806
R44	10k	Chip	0.125	5	20-5768
R45	8.2k	Chip	0.125	5	20-5767
R46	1k	Chip	0.125	5	20-5792
R47	1M	Chip	0.125	5	20-5770
R48	100k	Chip	0.125	5	20-5813
R49	10M	Carbon Film	¼	10	20-2106
R50	150	Carbon Film	½	5	20-3151
R51	10k	Chip	0.125	5	20-5768

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
	F		V		
C1	330n	Electrolytic	50		21-0793
C2	10µ	Electrolytic	16		21-0775
C3	100n	Ceramic			21-1708
C4	100n	Ceramic			21-1708
C5	220p	Chip			21-1838
C6	330n	Electrolytic	50		21-0793
C7	10n	Chip			21-1801
C8	1.5µ	Electrolytic	50		21-0787
C9	33n	Ceramic			21-1547
C10	22µ	Electrolytic	16		21-0776
C11	33µ	Electrolytic	25		21-0782
C12	100n	Electrolytic	50		21-0778
C13	10n	Ceramic			21-1752
C14	100n	Electrolytic	50		21-0778
C15	330µ	Electrolytic	40		21-0687
C16	100n	Ceramic			21-1708
C17	100n	Ceramic			21-1708
C18	10µ	Electrolytic	16		21-0716
C19	10µ	Electrolytic	16		21-0716
C20	10n	Chip			21-1801
C21	10n	Chip			21-1801
C22	10n	Chip			21-1801
C23	47µ	Electrolytic	16		21-0788
C24	47µ	Electrolytic	16		21-0788
Diodes					
D1		Silicon (1N4002)			22-1602
D2		Silicon (1N4149)			22-1029
D3		Silicon (1N4149)			22-1029
D4		Silicon (1N4149)			22-1029
D5		Silicon (1N4149)			22-1029

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D6		Silicon (1N4149)			22-1029
D7		Avalanche (BYV95A)			22-2009
D8		Avalanche (BYV95A)			22-2009
D9		Schottky (MBR340P)			22-2008
D10		Schottky (MBR340P)			22-2008
D11		Voltage Regulator (BZX79B3V9)			22-1825
D12		Silicon (1N4002)			22-1602
D13		Voltage Regulator (BZX79B5V6)			22-1856
D14		Silicon (1N4149)			22-1029
D15		Silicon (1N5401)			22-2010
Transformers					
T1					17-4104
Transistors					
Q1		2N3904			22-6007
Q2		2N3906			22-6008
Q3		2N3904			22-6007
Q4		2N3906			22-6008
Q5		BUZ21			22-6208
Q6		2N3904			22-6007
Q7		MJE371			22-6139
Q8		2N3904			22-6007
Q9		2N3904			22-6007
Q10		BDT92			22-6153
Integrated Circuits					
IC1		4072			22-4770
IC2		4030			22-4729
IC3		4001			22-4738
IC4		CA358E			22-4295
IC5		4001			22-4738
IC6		LM339N			22-4249
IC7		LAS6320P			22-4291
IC8		78L05			22-4247

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
SK21		Connector 24-way (Less Keyways)			23-5169
SK21		Keyways			23-5500
Miscellaneous					
RLA		Relay			23-7531
SWITCH BOARD ASSEMBLY 19-1242					
Resistors	Ω		W		
R1	100k	Chip	0.125	5	20-5813
R2	10k	Chip	0.125	5	20-5768
R3	10k	Chip	0.125	5	20-5768
R4	100k	Chip	0.125	5	20-5813
R5	1k	Chip	0.125	5	20-5792
R6	1k	Chip	0.125	5	20-5792
R7	10k	Chip	0.125	5	20-5768
R8	100k	Chip	0.125	5	20-5813
R9	10k	Chip	0.125	5	20-5768
R10	10k	Chip	0.125	5	20-5768
Capacitors			V		
C1	200µ	Electrolytic	40		21-0686
C2	100n	Ceramic			21-1708
Diodes					
D1		Silicon (1N4002)			22-1602
D2		Schottky (MBR340P)			22-2008

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
Q1		2N3904			22-6007
Q2		2N3906			22-6008
Q3		2N3906			22-6008
Q4		2N3906			22-6008
Q5		2N3906			22-6008
Miscellaneous					
JK1		Socket			23-3433
S1		Switch SPDT			23-4126
S2		Switch DPDT			23-4127
FS1		Fuselink 1¼ in x ¼ in	3AT		23-0069
		Fuseholder for FS1			23-0062
		Top for 23-0062			23-0063



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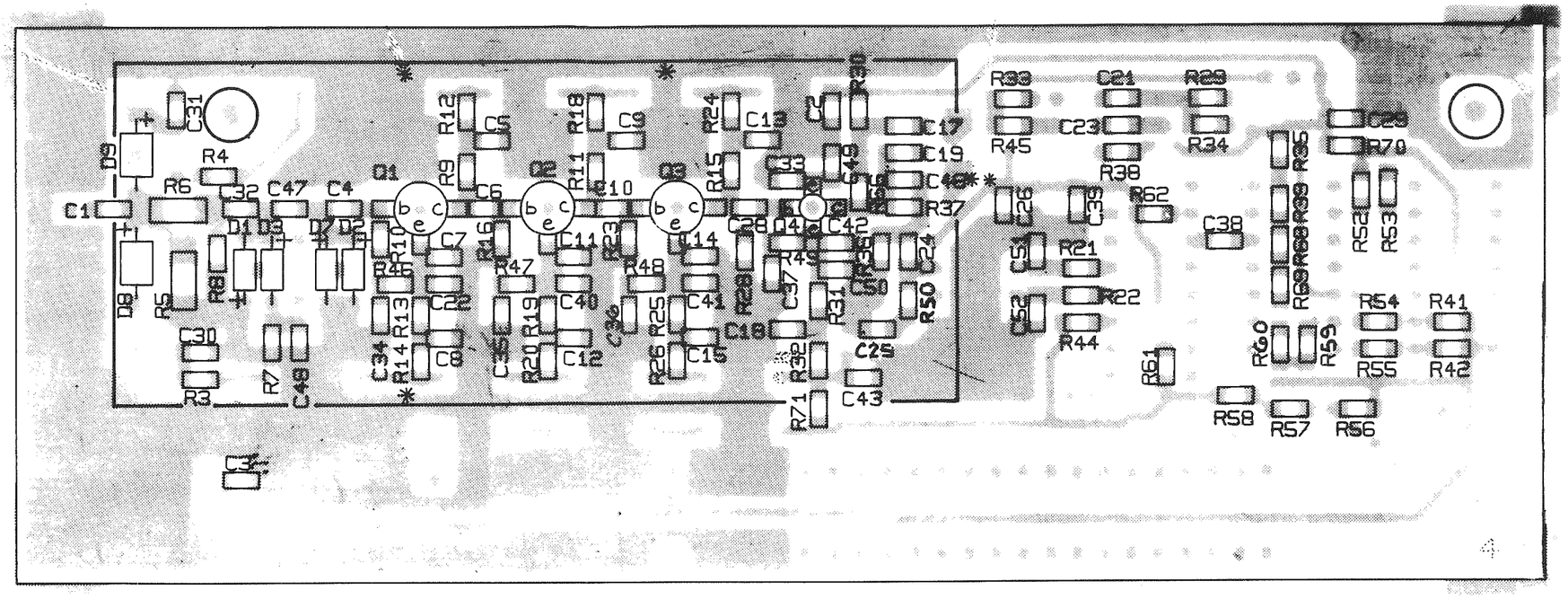
YH7296

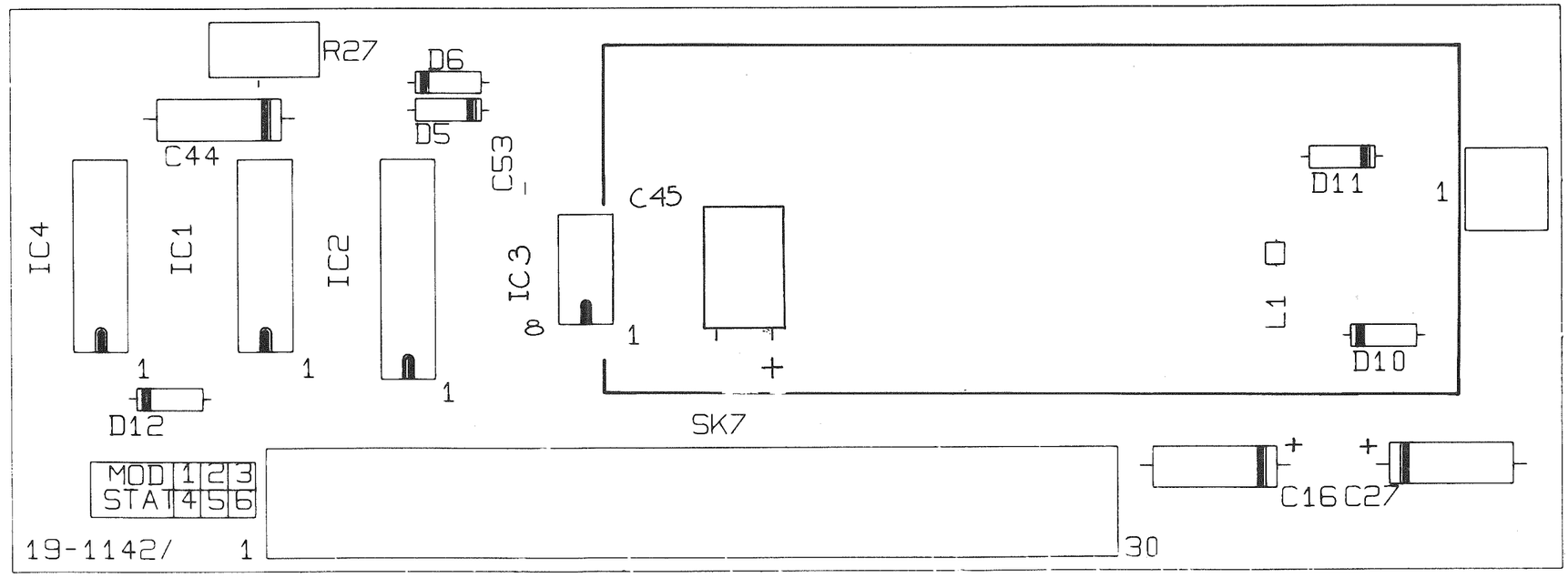
Internal Layout

Fig.1

TRACKSIDE VIEW



COMPSIDE VIEW



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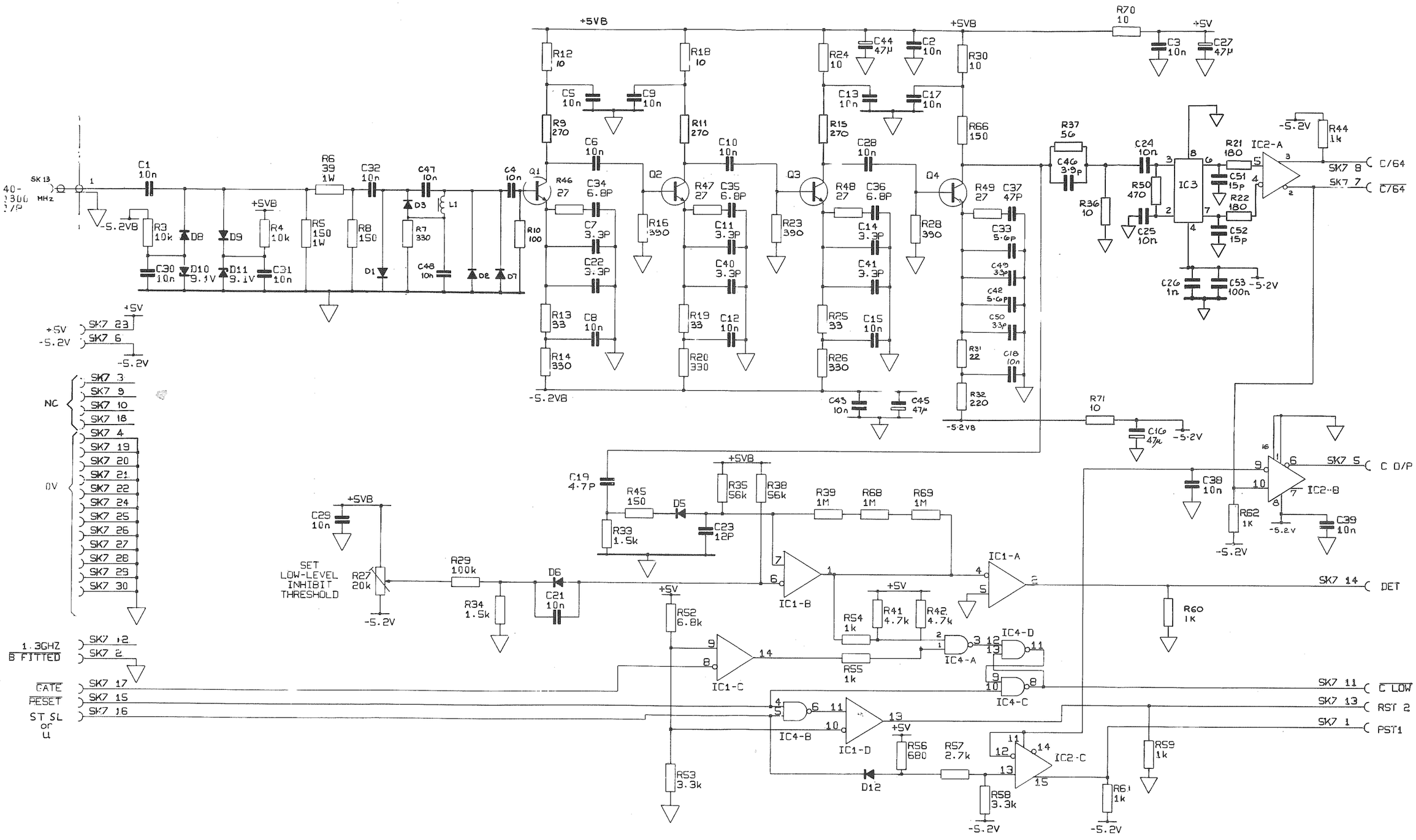
TH7296
4

Component Layout:
Channel B Assembly 19-1142 Fig. 2



RACAL
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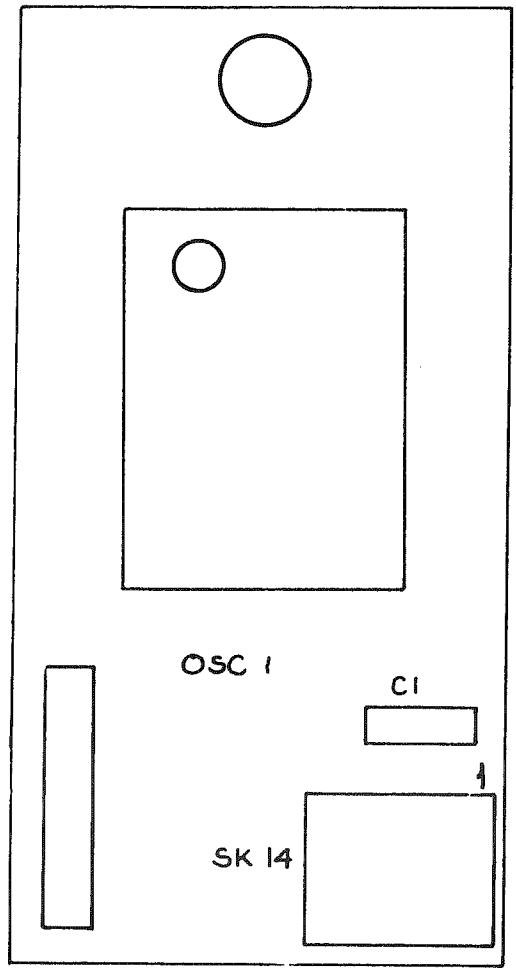
3

Circuit Diagram:
Channel B Assembly 19-1142

Fig.3



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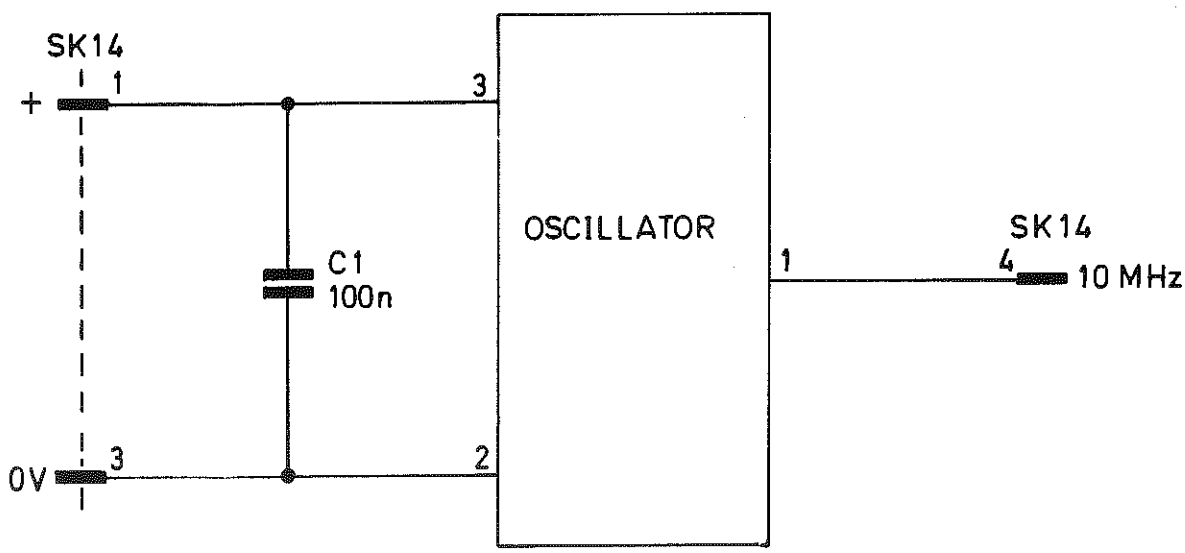
1

Component Layout:
Oscillator Assembly 19-1147

Fig. 4



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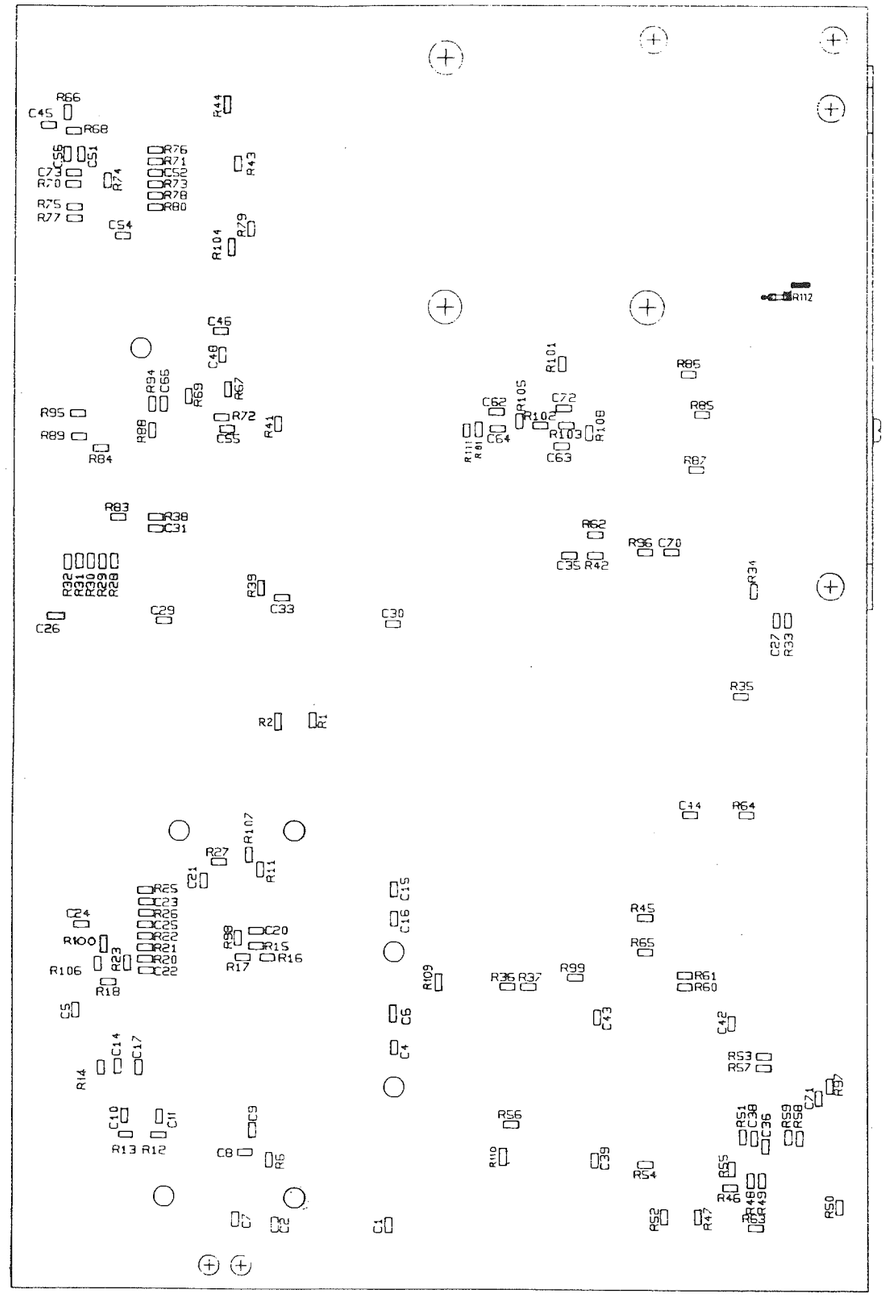
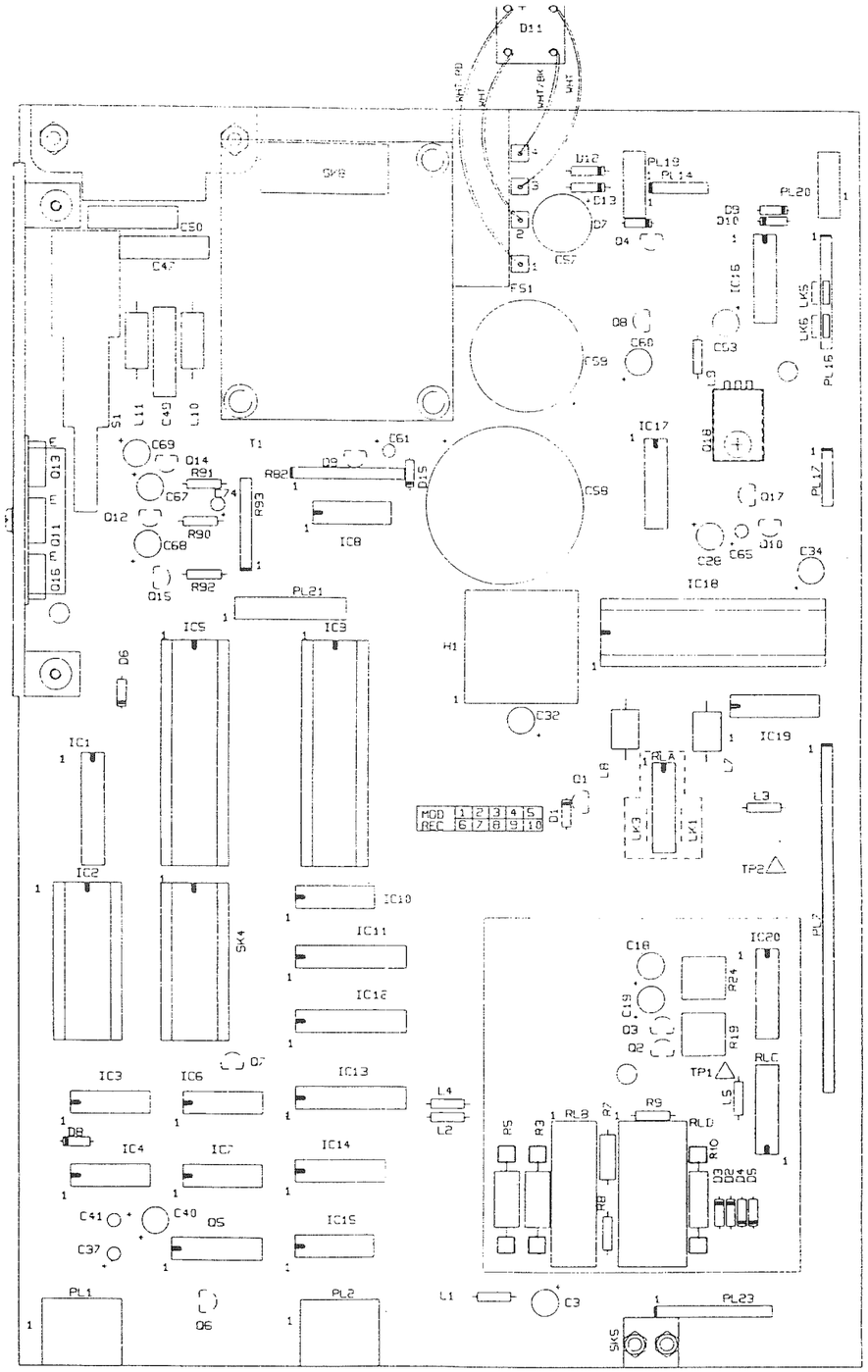
1

Circuit Diagram
Oscillator Assembly 19-1147

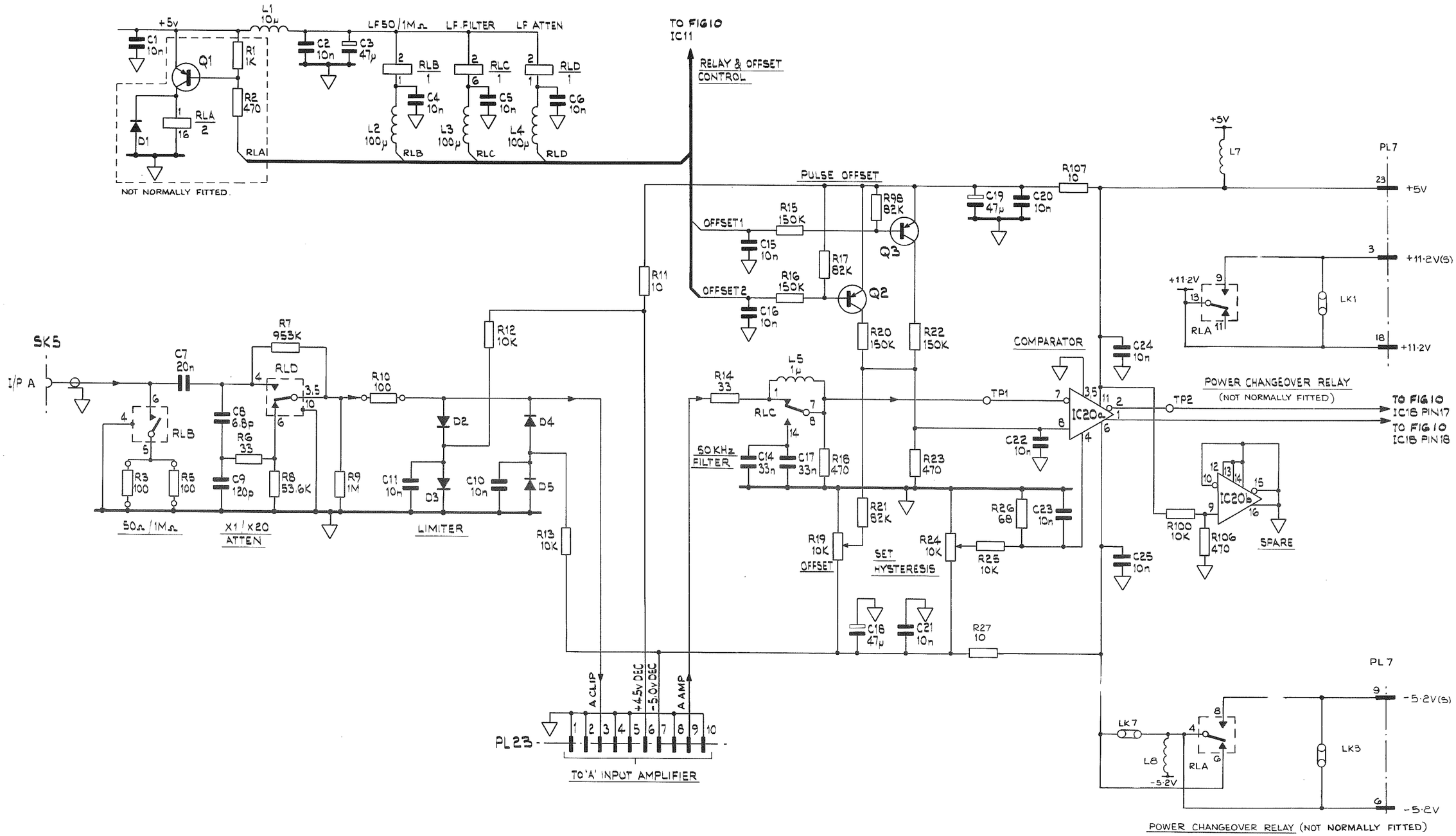
Fig.5





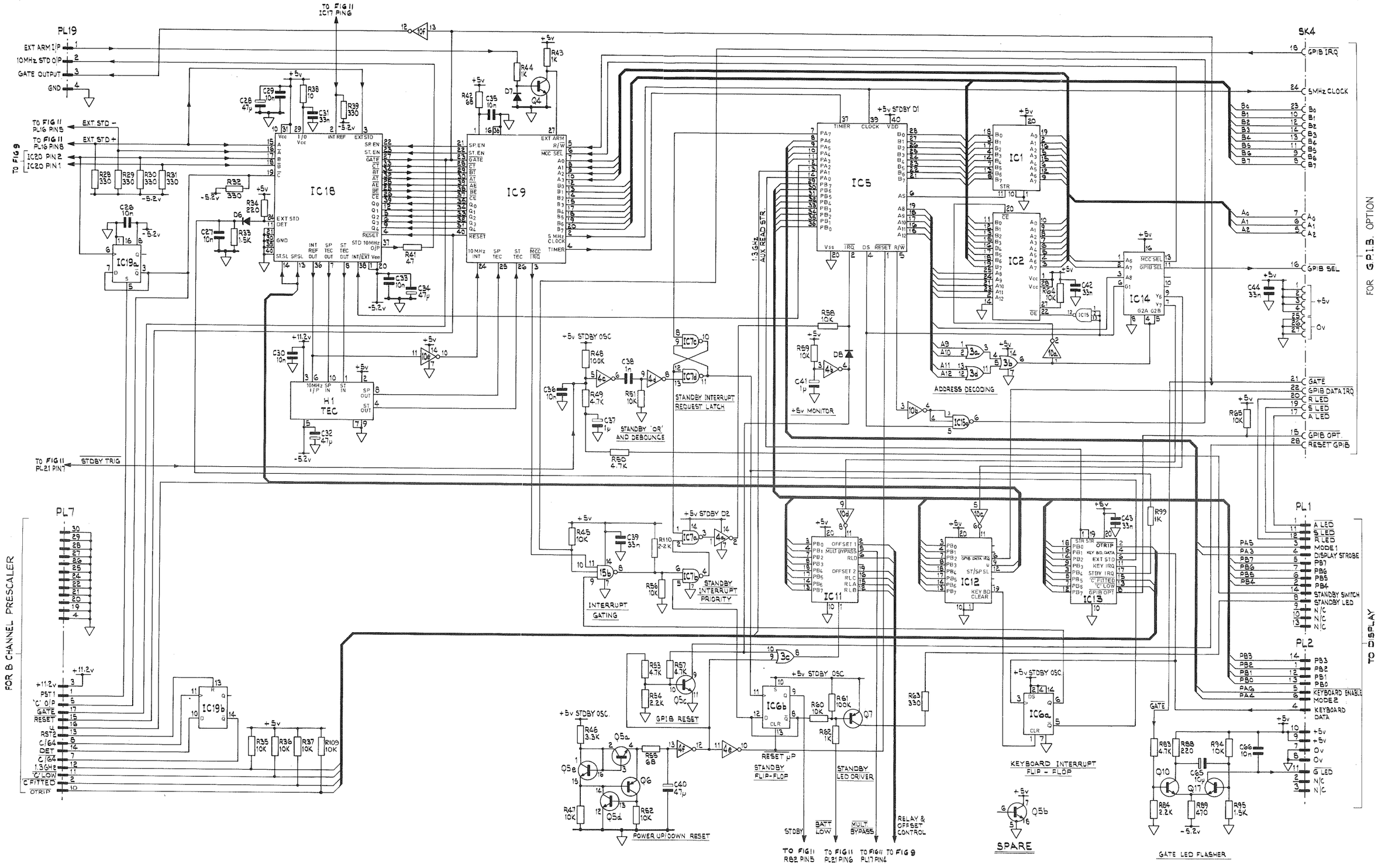
RACAL
TH7296
1|2|3

Component Layout:
Motherboard Assembly 19-1160 Fig.6



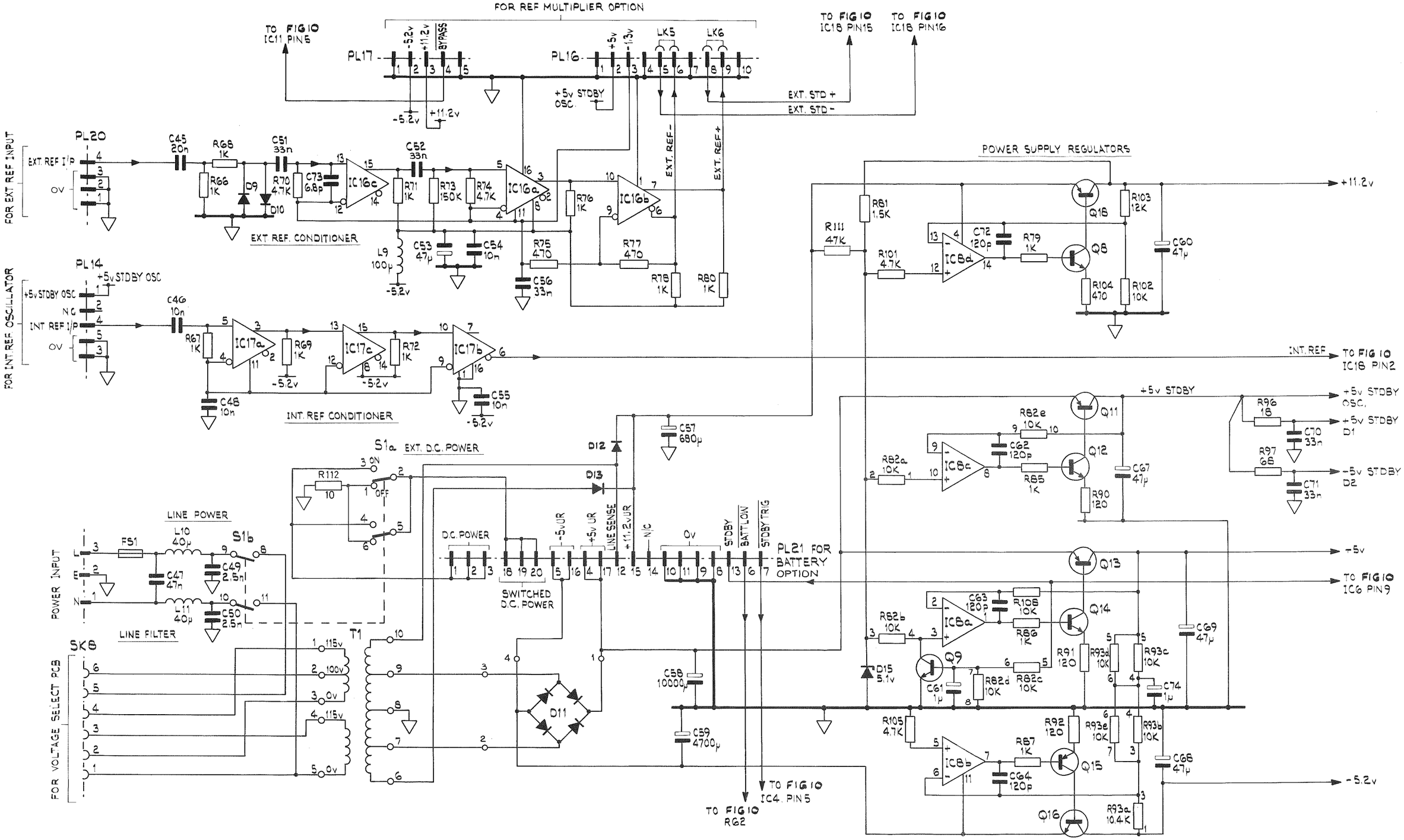
RACAL
TH 7296
1|2

Circuit Diagram: Motherboard Assembly 19-1160 **Fig.7**



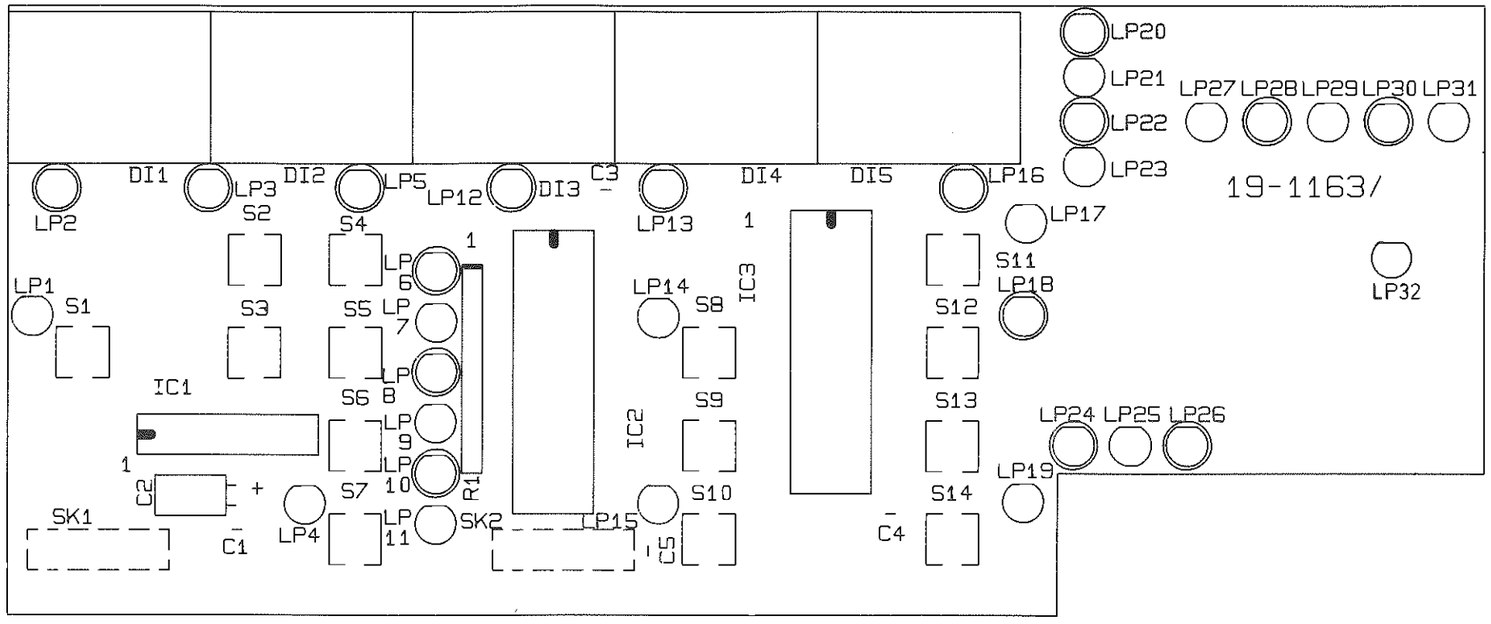
RACAL
TH7296
1|2

Circuit Diagram:
Motherboard Assembly 19-1160 Fig. 8



RACAL
TH7296
1 2 3 4

Circuit Diagram:
Motherboard Assembly 19-1160 Fig.9



RACAL
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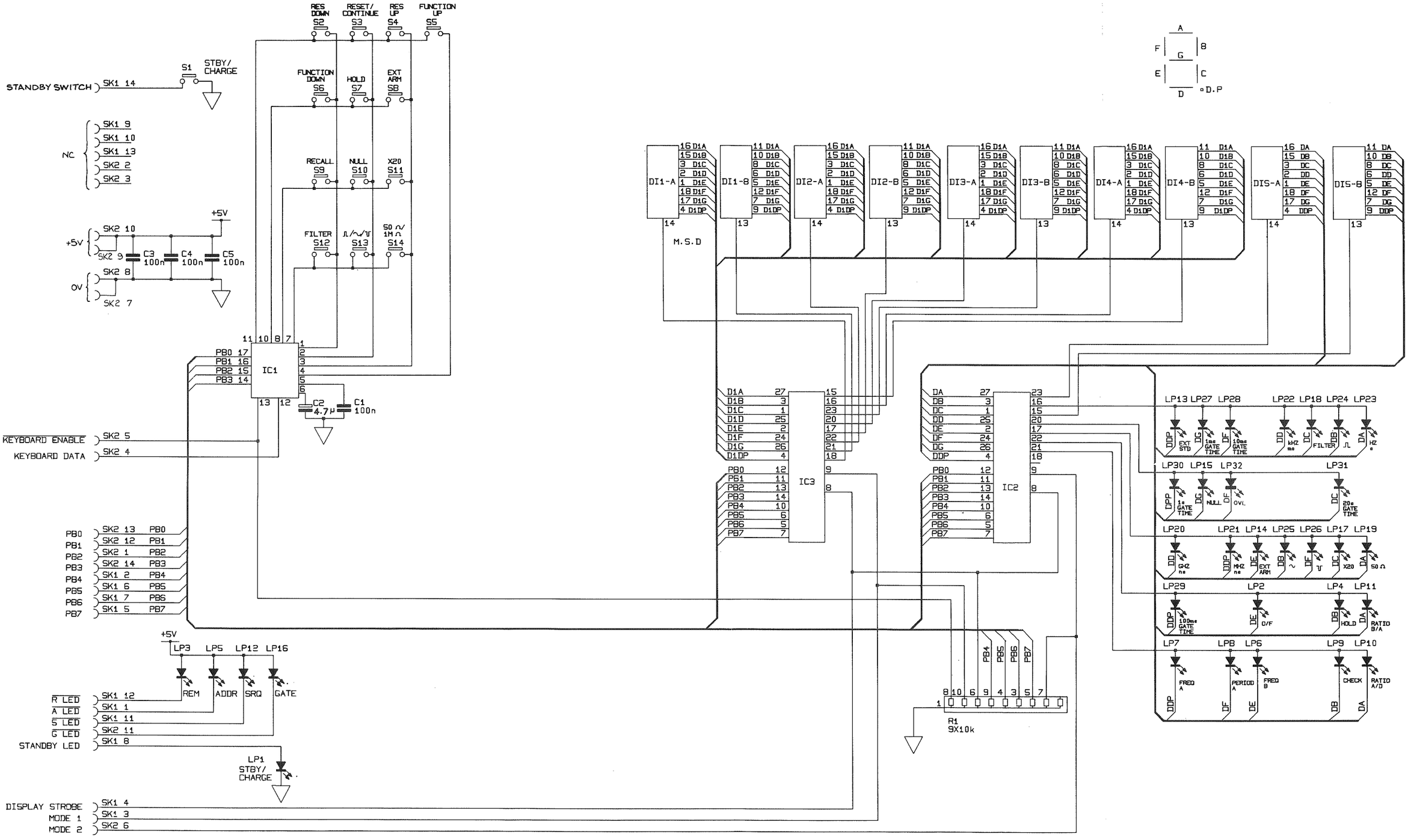
1|2

Component Layout:
Display Assembly 19-1163

Fig.10



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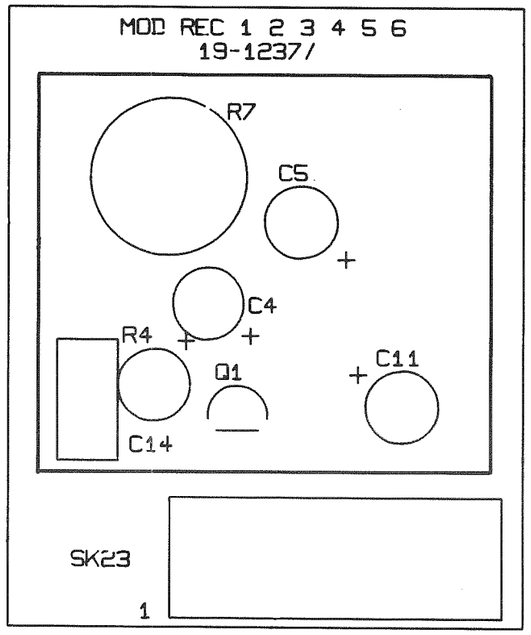
1|2

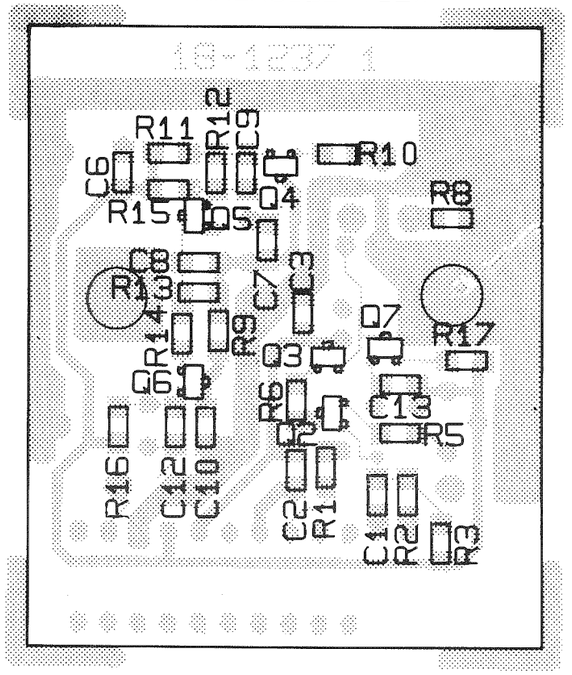
Circuit Diagram:
Display Assembly 19-1163

Fig.11

COMPSIDE VIEW



TRACKSIDE VIEW



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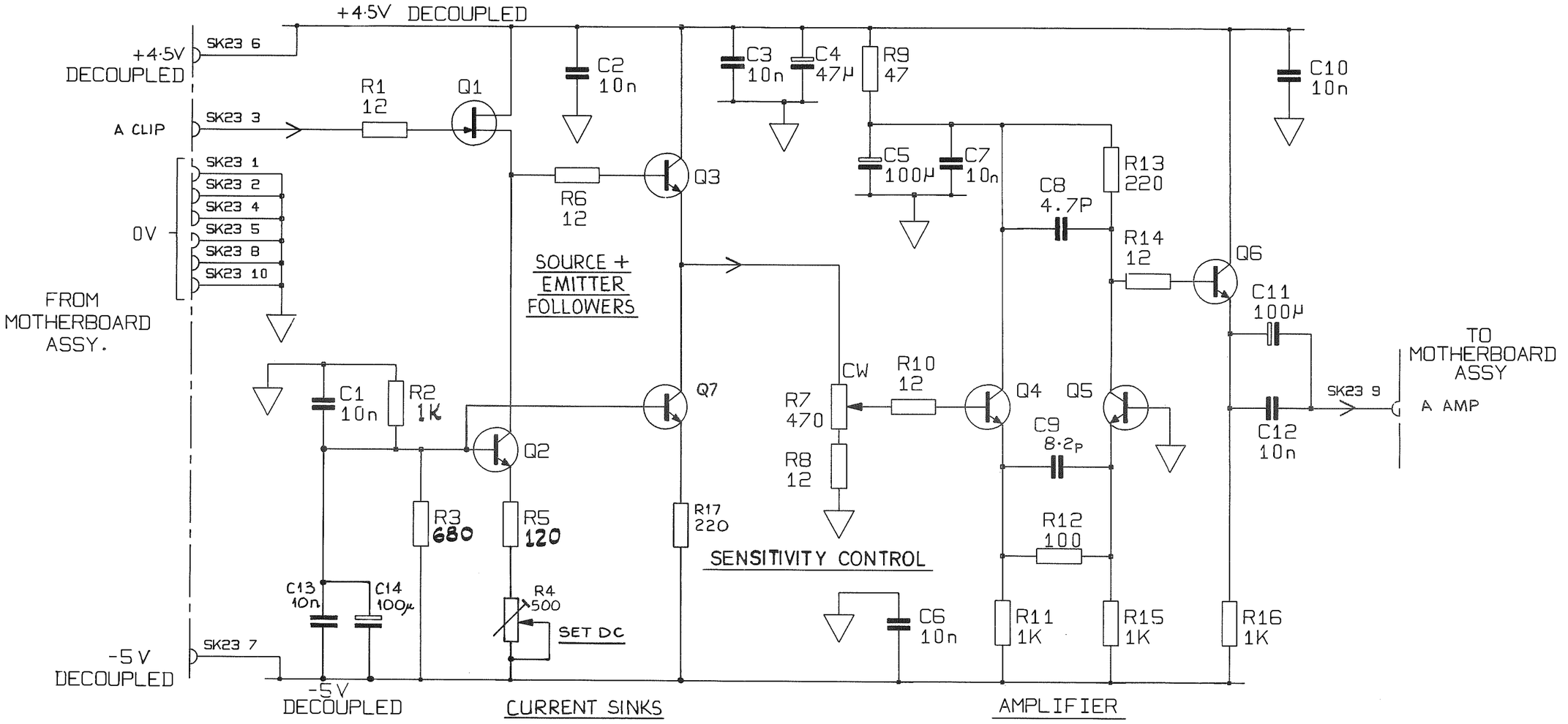
Component Layout: Input A
Amplifier Assembly 19-1237

Fig. 12



RACAL
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1 2

Circuit Diagram: Input A
Amplifier Assembly 19-1237

Fig. 13

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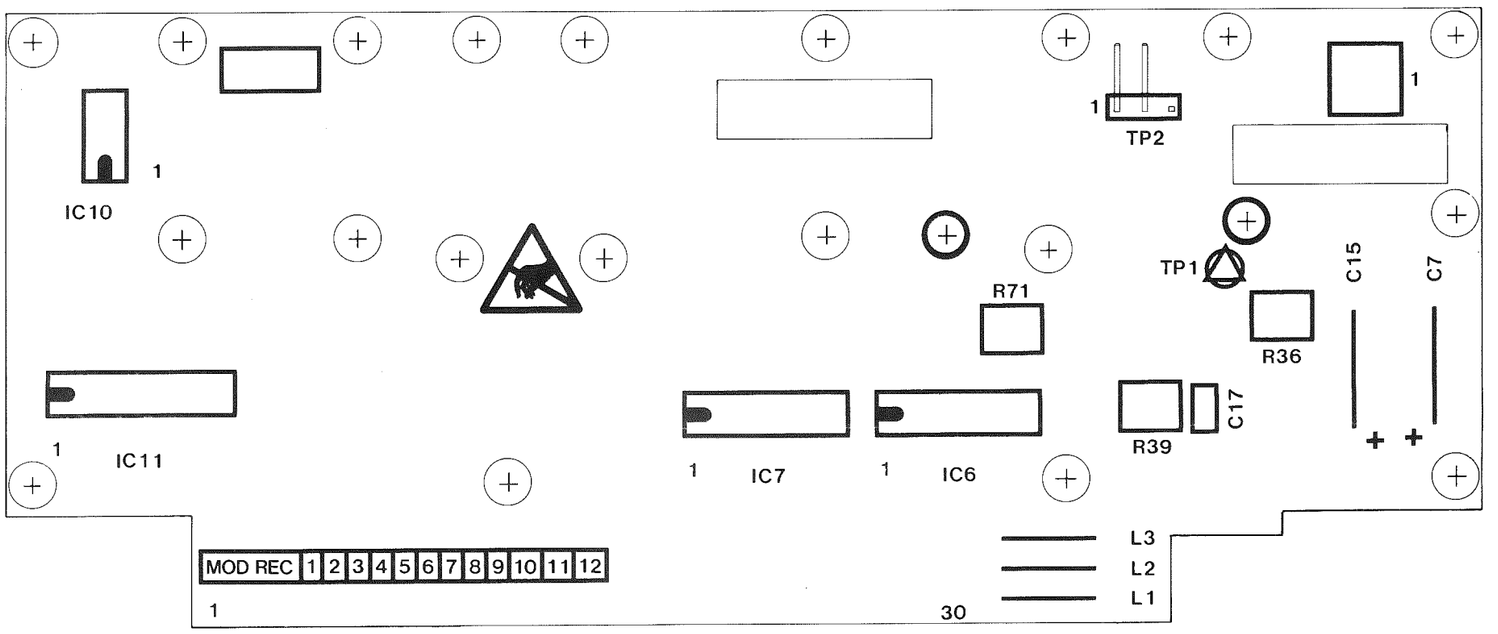
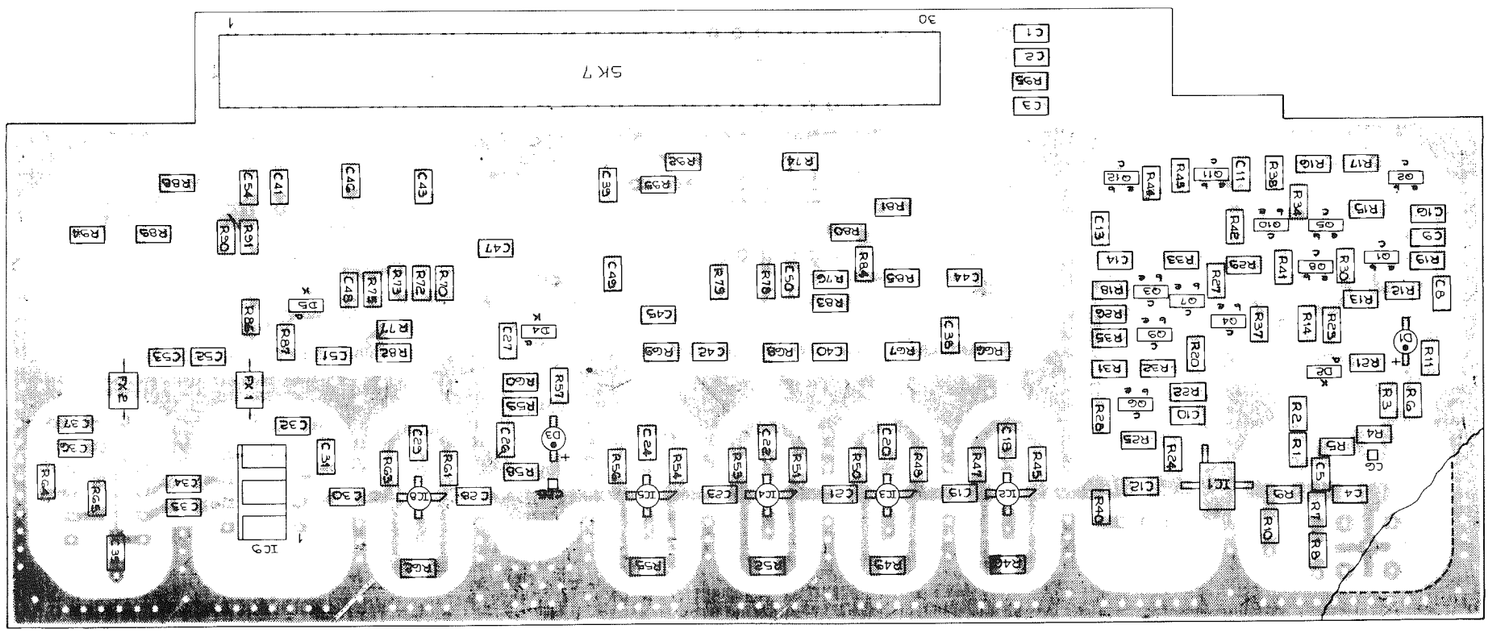




Component Layout:
Channel B Assembly 19-1300 Fig.14

PIN DIODE T ATTENUATOR

I/P 80-2600 MHz

2-6GHz AMPLIFIER (8dB PER STAGE)

+4 & -64 PRESCALER IC'S

OVERLOAD SETUP D.C I/P

SET LOW-LEVEL INHIBIT THRESHOLD

SET AGC THRESHOLD

SET OVERLOAD THRESHOLD

T ATTENUATOR CONTROL CIRCUIT

DETECTOR LOGIC SYNCHRONISING CIRCUIT

SK7

C FITTED

1·3GHz / 2·6GHz

0V

KEY

C/64

C/64

C O/P

OET.

C' LOW

GATE

RESET

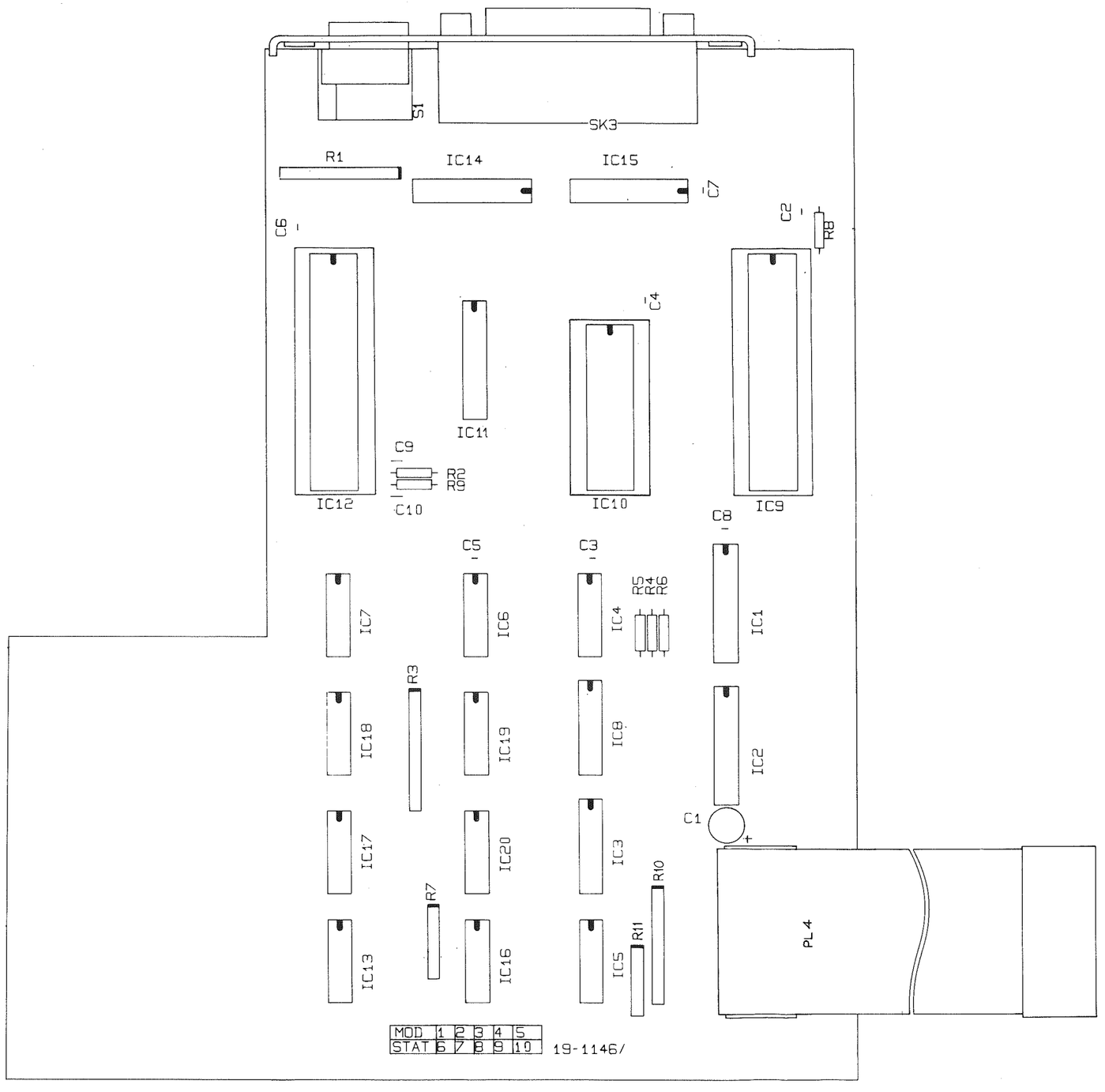
RST 2

PST 1

U

O TRIP

Circuit:
Channel B Assembly 19-1300 Fig.15



Component Layout:
GPIB Assembly 19-1146

Fig.16

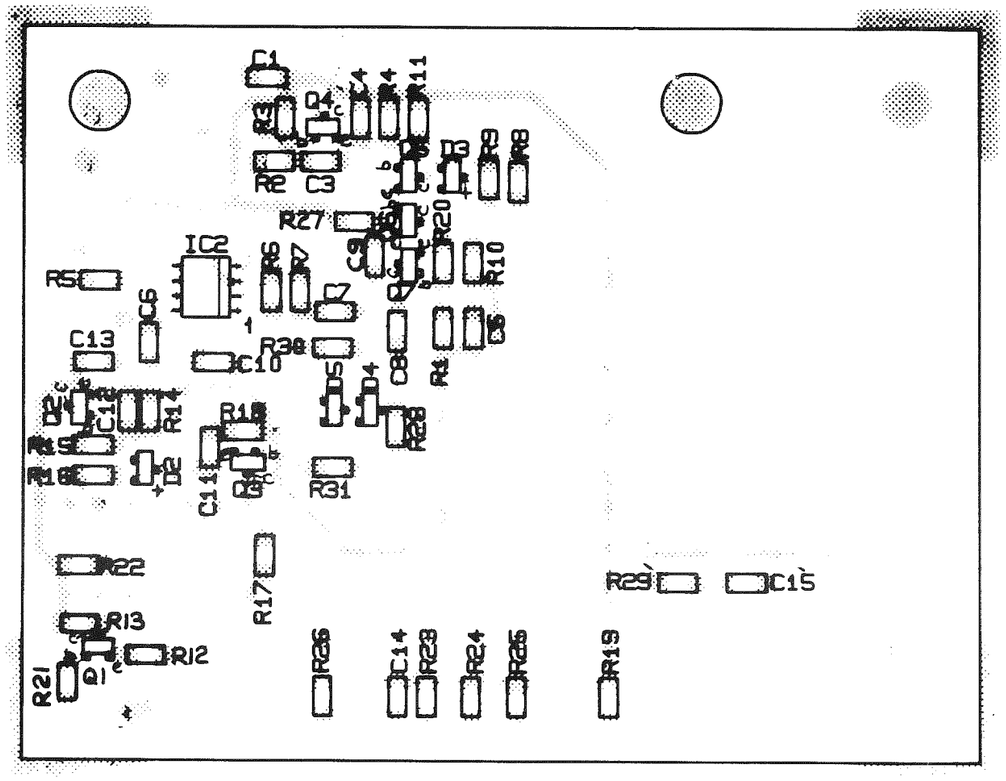
NOTE; SIGNALS ON SK3 ARE NEGATIVE LOGIC

Circuit Diagram:
GPIB Assembly 19-1146

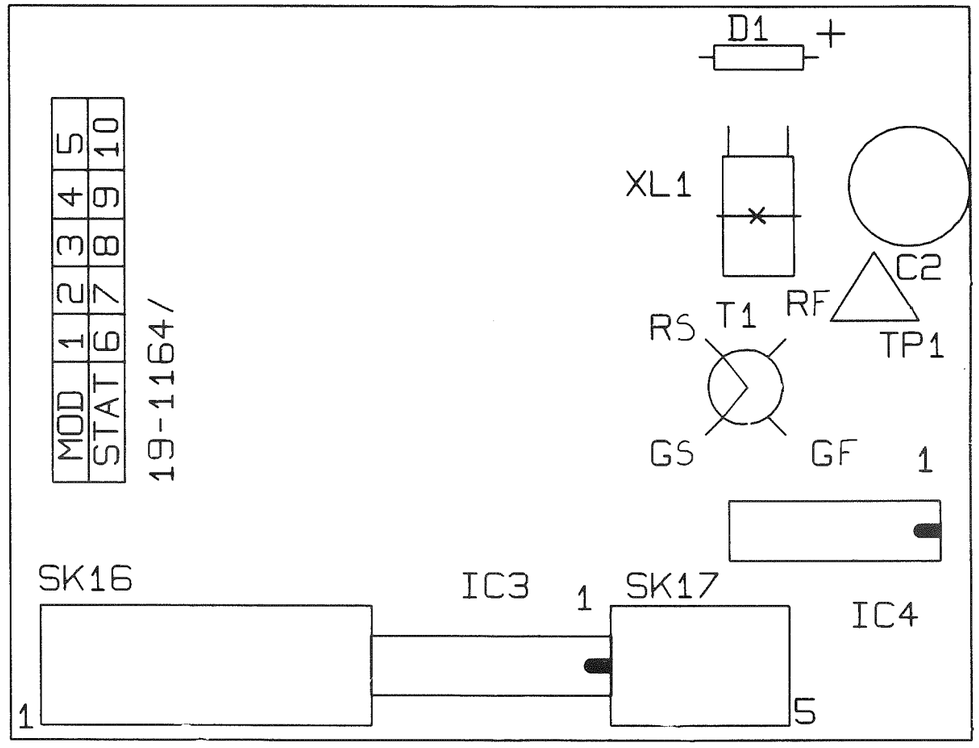
Fig.17

RACAL
TH7296
2 3

TRACKSIDE VIEW



COMPONENT SIDE VIEW



RACAL

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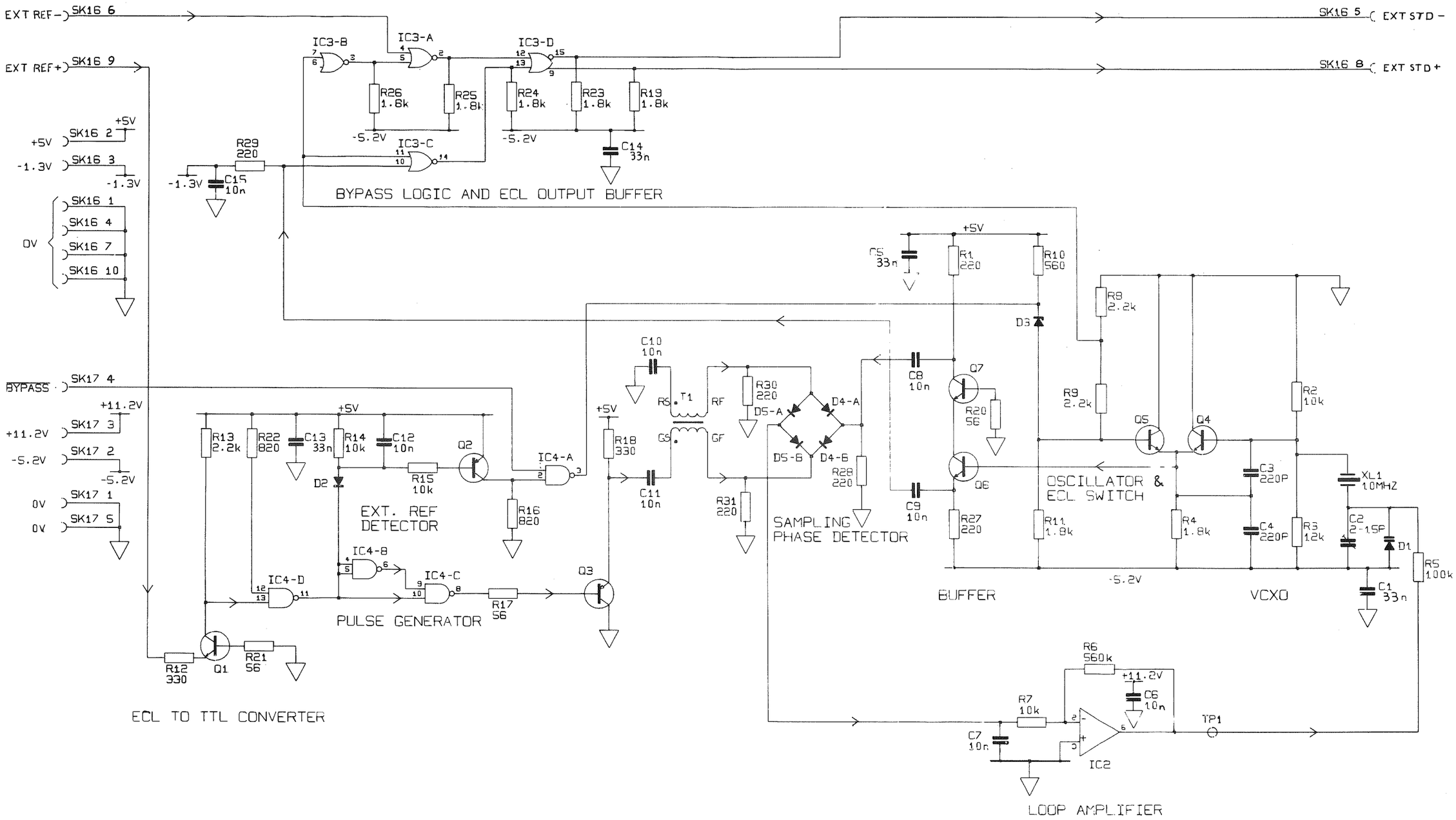
2

Component Layout: Reference Frequency Multiplier Assembly 19-1164 Fig. 18



RACAL
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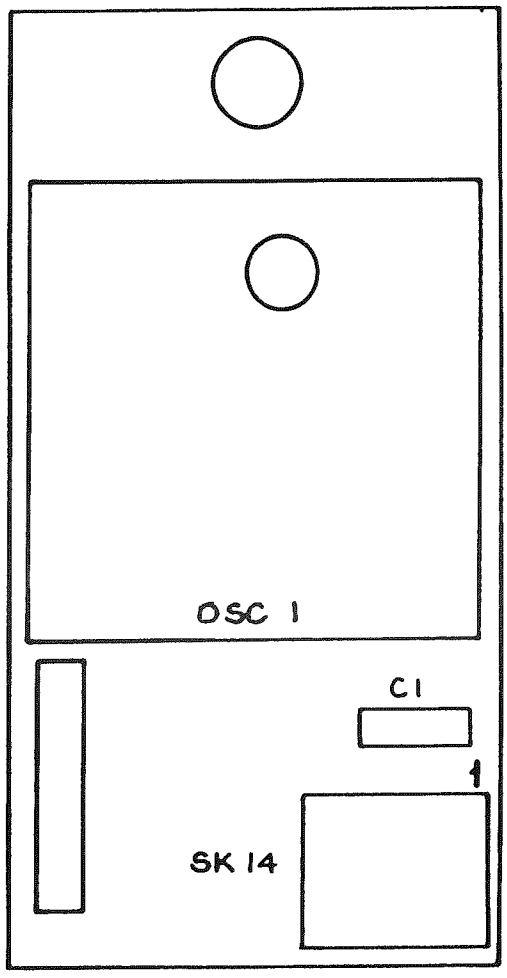
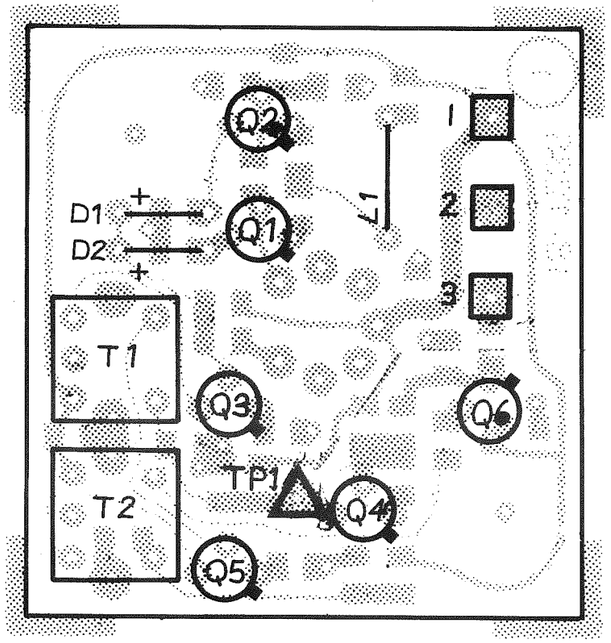
2

Circuit Diagram: Reference Frequency Multiplier Assembly 19-1164 Fig.19

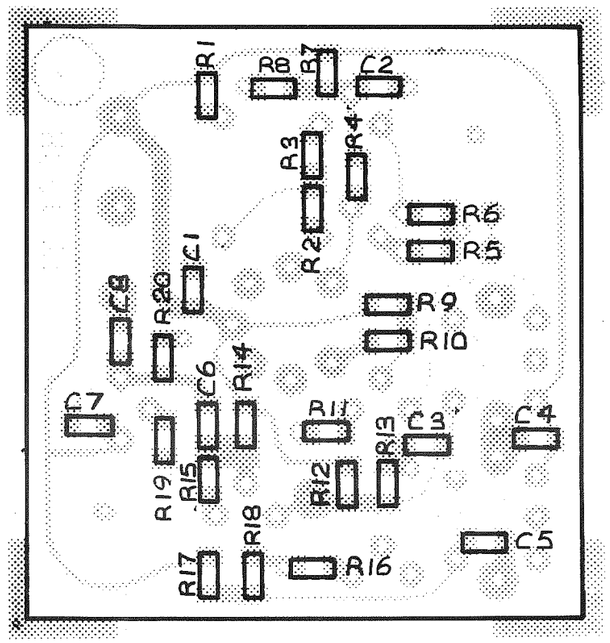


Component Layout:
Oscillator Assembly 19-1208

Fig.20



VIEWED FROM COMPONENT SIDE



VIEWED FROM TRACK SIDE

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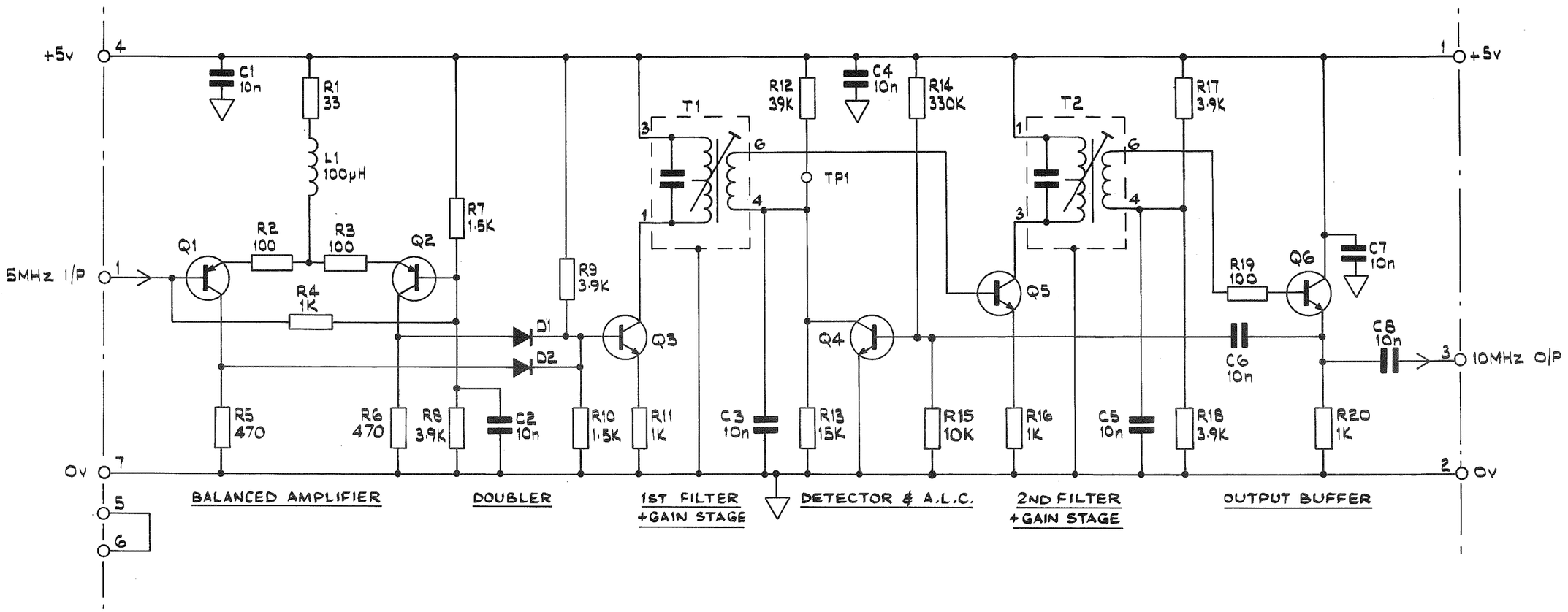
1

Component Layout: Reference Frequency
Doubler Assembly 19-1238 Fig.21



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1

Circuit Diagram: Reference Frequency
Doubler Assembly 19-1238 Fig.22

19-1203
BATTERY BD. ASSY

SK21
SWITCHED DC POWER
KEY

MANAGEMENT CIRCUITS

PART OF POWER SWITCH S1a

STDBY

LINE SENSE

SK11
NORM S1
EXT S2a
INT
FS1 3.15A
11-16V D.C. JK1
D2
S2b
PART 19-1242 SWITCH BD. ASSY

SK/PL12
FS2 WH/BN
B1
WH/BL
BATTERY PACK
FS3 WH/RD
B2
WH/BK
RLA1
RLA2
RLA3
RLA4
11-1723

POWER-DOWN LATCH
PART 19-1242 SWITCH BD. ASSY

CHARGER
+5V UR
-5·2V UR
MOUNTED ON 11-1722

CONVERTER

T1
+11·2V UR
+5V UR
-11·2V UR
-5V UR
0V
-5·2V UR
KEY
KEY

STBY TRIG
BATT LOW

SK21
PL21 (MOTHERBOARD)

NOTE:
20-PIN PLUG PL21 ON MOTHERBOARD CONNECTS TO SK21 AS SHOWN. TO CONVERT PL21 NUMBERS TO SK21 NUMBERS :-

TO PL21 PINS 1 TO 10, ADD 1
TO PL21 PINS 11 TO 20 ADD 3

RACAL
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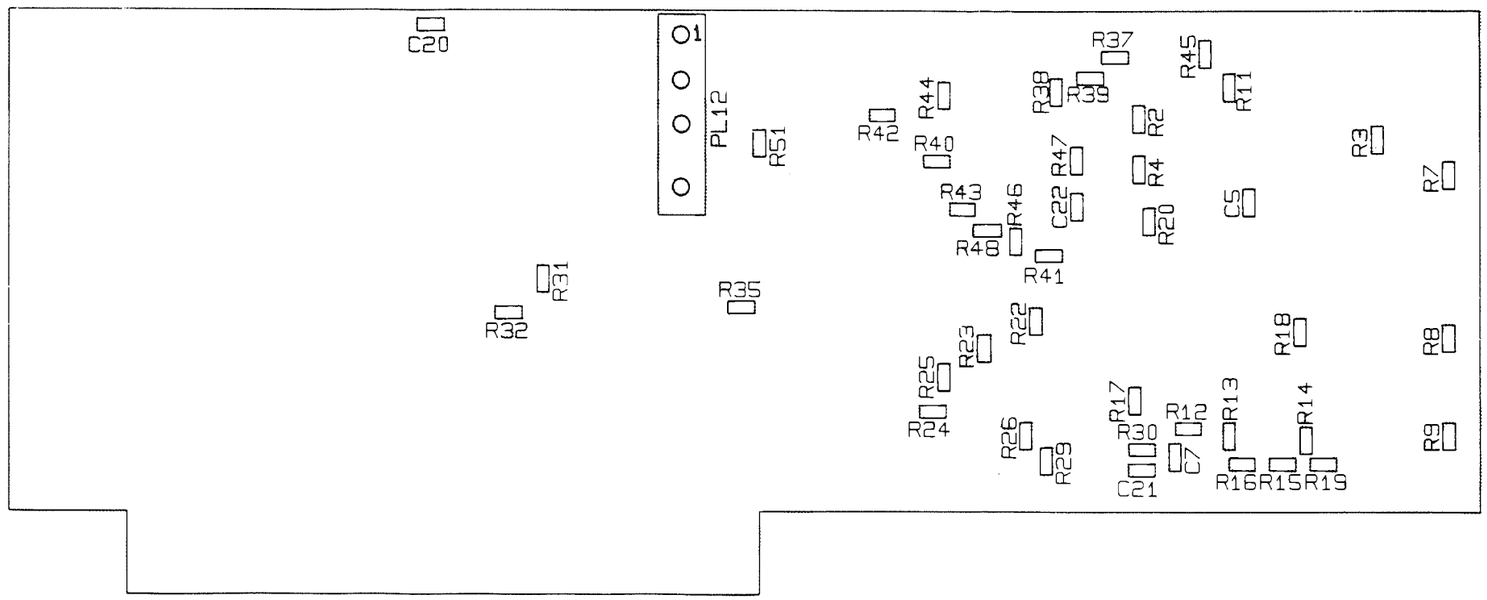
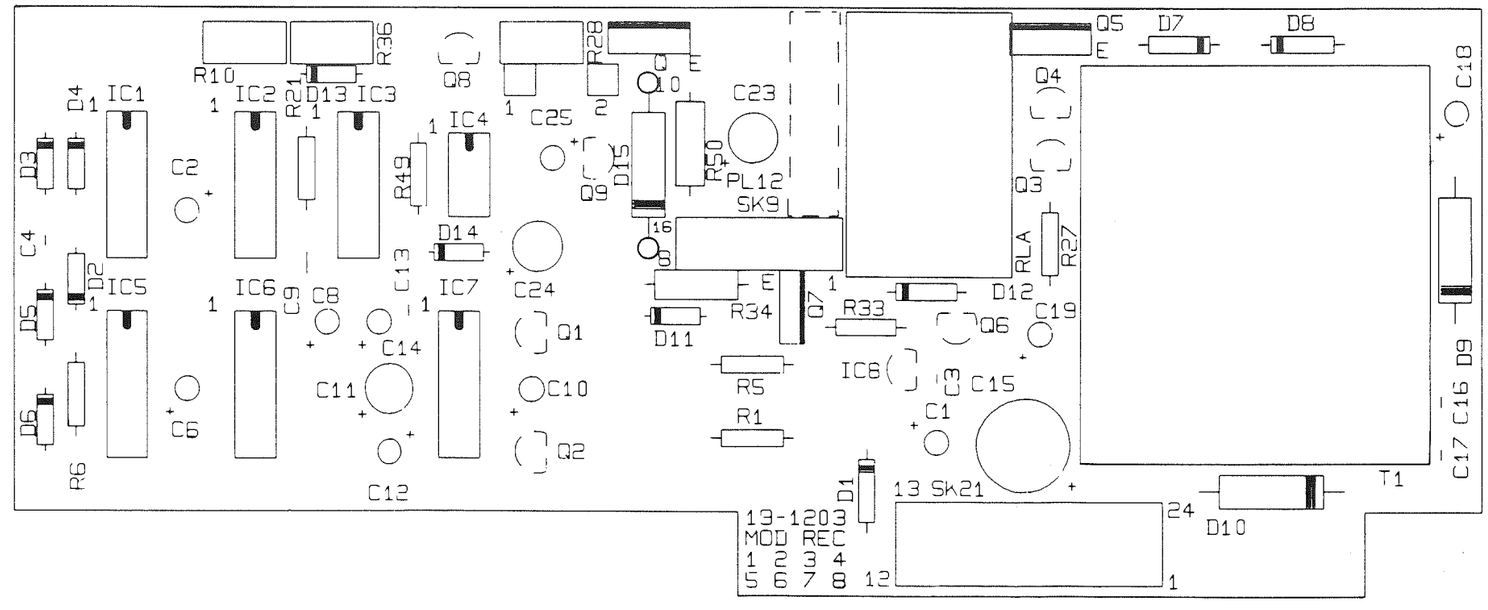
1

Circuit Diagram:
Battery Pack Assembly 11-1625 Fig.23



TRACKSIDE VIEW



COMPONENT SIDE VIEW

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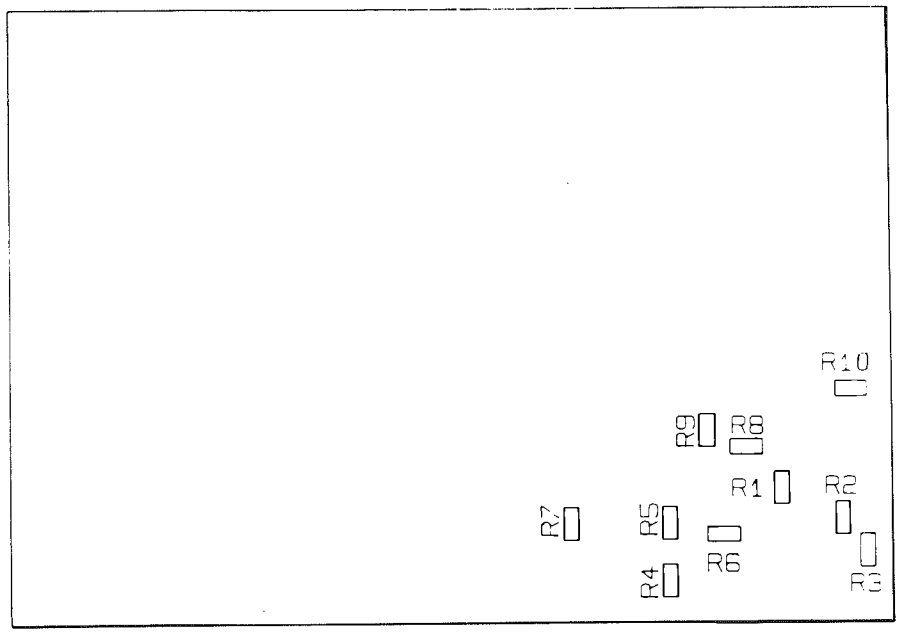
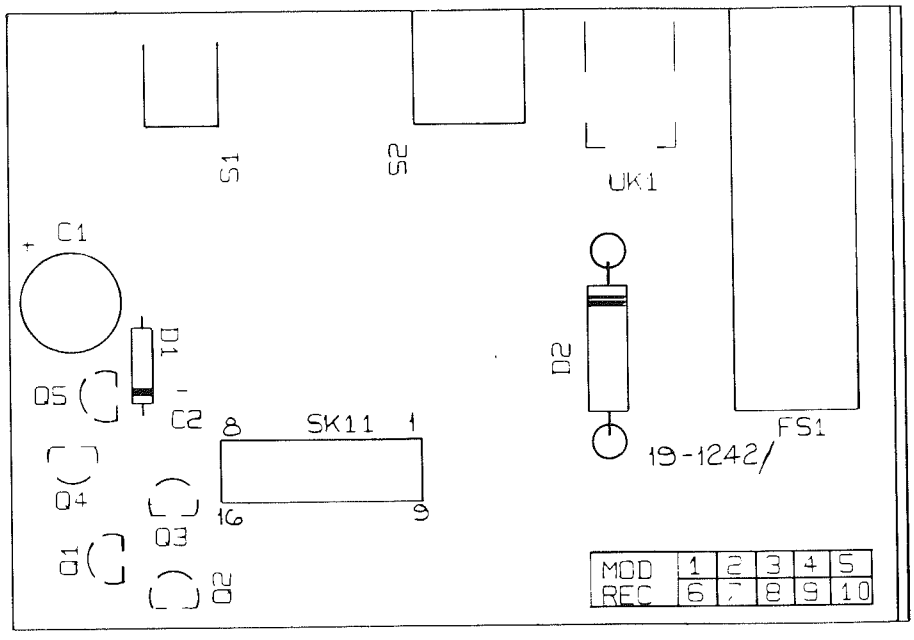
1

Component Layout:
Battery Board Assembly 19-1203 Fig.24



TRACKSIDE VIEW



COMPONENT SIDE VIEW

Component Layout :
Switch Board Assembly 19-1242

Fig. 25

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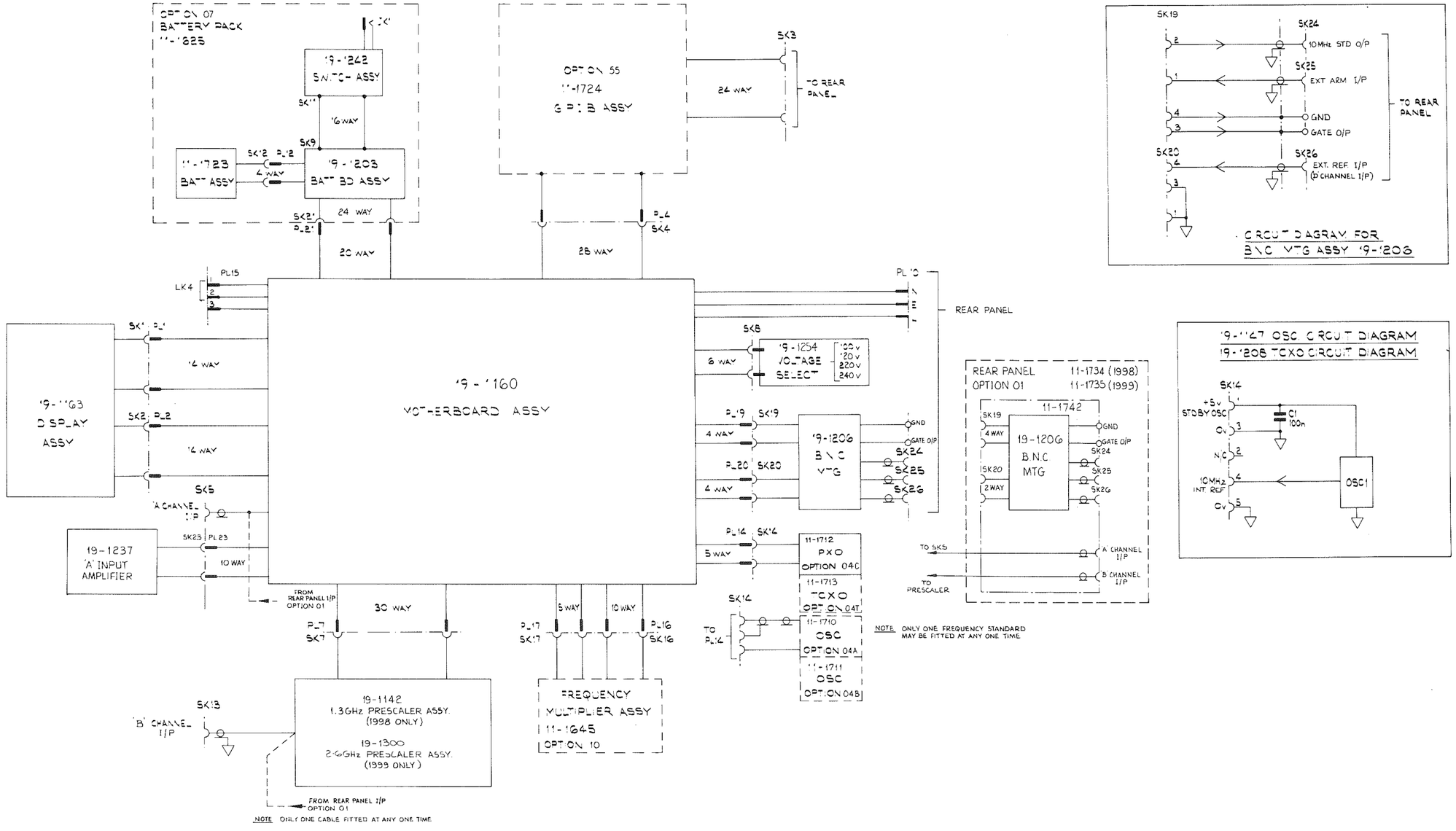
1



14 WAY	PL/SK 1
	PIN
STBY SWITCH	14
PB4	2
PB5	6
PB6	7
PB7	5
R LED	12
A LED	1
S LED	11
STBY LED	8
DISPLAY STROBE	4
MODE 1	3

14 WAY	PL/SK 2
	PIN
0V	7, 8, 9, 10
+5V	14
KEYBOARD ENABLE	5
KEYBOARD DATA	4
PB0	13
PB1	12
PB2	11
PB3	16
MODE2	6
GLED	11

24 WAY	SK3
	PIN
0V	12, 18, 19, 20, 21, 22, 23, 24
+5V	7
+12V	1
DAV	6
SRQ	10
NDAC	8
REN	17
EOI	5
IFC	9
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16

28 WAY	SK/PL 4
	PIN
+5V	1, 2, 3, 4
0V	25, 26, 27
RESET GPIB	28
5MHz CLOCK	24
GATE	21
GPIB OPT	15
B0	23
B1	10
B2	12
B3	14
B4	13
B5	11
B6	9
B7	8
AC	7
A1	6
A2	5
GPIB SEL	16
GPIB DATA IRQ	22
GPIB IRQ	18
R LED	20
A LED	17
S LED	19

4 WAY	PL/SK 12
	PIN
BATTERY 1 0V	3
BATTERY 1 +6V	1
BATTERY 2 +6V	4
BATTERY 2 0V	2

10 WAY	PL/SK 23
	PIN
0V	1, 2, 4, 5, 8, 10
A CLIP	3
+4.5V DEC	6
-5V DEC	7
A AMP	9

30 WAY	PL7	SK7 1998 ONLY	SK7 1999 ONLY
	PIN	PIN	PIN
+5V	23	23	23
-5.2V	6	6	6
0V	4, 9-22, 24-26, 28-30	4, 19-22, 24-26, 28-30	14-26, 28-30
1.3GHz	12	12	12
GATE	17	17	17
RESET	15	15	15
LI	16	16	16
C/64	8	8	8
C/64	7	7	7
C/20	5	5	5
DET	14	14	14
CLOW	11	11	11
RST2	13	13	13
RST1	1	1	1
C FITTED	2	2	2
+11.2V(S)	3		3
OTRIP	10		10
+11.2V	18		18
-5.2V(S)	9		9

16 WAY	SK9, 11
	PIN
0V	4, 5, 6, 12
NORM/BS	14
EXT/INT	13
POWER EXT/INT	1, 2, 3
BATTERY	9, 10, 11

5 WAY	PL/SK 14
	PIN
+5V STDBY OSC	1
0V	3, 5
10 MHz INT REF	4

10 WAY	PL16	SK16
	PIN	PIN
+5V STDBY OSC	2	2
-1.3V	3	3
0V	1, 4, 7, 10	1, 4, 7, 10
EXT REF -	6	6
EXT REF +	9	9
EXT STD +	5	5
EXT STD -	8	8

5 WAY	PL/SK 17
	PIN
+11.2V	3
-5.2V	2
0V	1, 5
BYPASS	4

PL19 - 4 WAY SK19 - 4 WAY	PL19	SK19
	PIN	PIN
10MHz STD O/P	2	2
EXT ARM	1	1
0V	4	
GATE O/P	3	3

4 WAY	PL/SK 20
	PIN
0V	1, 2, 3
EXT REF.	4

PL21 - 20 WAY SK21 - 24 WAY	PL 21	SK 21
	PIN	PIN
DC POWER	1, 2, 3	1, 2, 3, 4
SWITCHED DC POWER	15, 19, 20	21-24
-5v UR	5, 16	6, 19
+5v UR	4, 17	5, 20
LINE SENSE	12	15
+11.2v UR	15	18
-11.2v UR		17
0V	8, 9, 10, 11	9-14
STDBY	13	16
BATT LOW	6	7
STDBY TRIG	7	8

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1 | 2 | 3